Digital Modulation

CHAPTER OUTLINE

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OBJECTIVES

- Define *electronic communications*
- Define *digital modulation* and *digital radio*
- Define *digital communications*
- Define *information capacity*
- Define *bit, bit rate, baud,* and *minimum bandwidth*
- Explain Shannon's limit for information capacity
- Explain *M*-ary encoding
- Define and describe digital amplitude modulation
- Define and describe frequency-shift keying
- Describe continuous-phase frequency-shift keying
- Define *phase-shift keying*
- Explain binary phase-shift keying
- Explain quaternary phase-shift keying
- Describe 8- and 16-PSK
- Describe quadrature-amplitude modulation
- Explain 8-QAM
- Explain 16-QAM
- Define *bandwidth efficiency*
- Explain carrier recovery
- Explain clock recovery
- Define and describe differential phase-shift keying
- Define and explain trellis-code modulation
- Define *probability of error* and *bit error rate*
- Develop error performance equations for FSK, PSK, and QAM

From Chapter 2 of *Advanced Electronic Communications Systems*, Sixth Edition. Wayne Tomasi.

1 INTRODUCTION

In essence, *electronic communications* is the transmission, reception, and processing of information with the use of electronic circuits. *Information* is defined as knowledge or intelligence that is communicated (i.e., transmitted or received) between two or more points. *Digital modulation* is the transmittal of digitally modulated analog signals (carriers) between two or more points in a communications system. Digital modulation is sometimes called *digital radio* because digitally modulated signals can be propagated through Earth's atmosphere and used in wireless communications systems. Traditional electronic communications systems that use conventional analog modulation, such as *amplitude modulation* (AM), *frequency modulation* (FM), and *phase modulation* (PM), are rapidly being replaced with more modern digital moduluation systems that offer several outstanding advantages over traditional analog systems, such as ease of processing, ease of multiplexing, and noise immunity.

Digital communications is a rather ambiguous term that could have entirely different meanings to different people. In the context of this text, digital communications include systems where relatively high-frequency analog carriers are modulated by relatively low-frequency digital information signals (*digital radio*) and systems involving the transmission of digital pulses (*digital transmission*). Digital transmission systems transport information in digital form and, therefore, require a physical facility between the transmitter and receiver, such as a metallic wire pair, a coaxial cable, or an optical fiber cable. In digital radio systems, the carrier facility could be a physical cable, or it could be free space.

The property that distinguishes digital radio systems from conventional analog-modulation communications systems is the nature of the modulating signal. Both analog and digital modulation systems use analog carriers to transport the information through the system. However, with analog modulation systems, the information signal is also analog, whereas with digital modulation, the information signal is digital, which could be computer-generated data or digitally encoded analog signals.

Referring to Equation 1, if the information signal is digital and the amplitude (V) of the carrier is varied proportional to the information signal, a digitally modulated signal called *amplitude shift keying* (ASK) is produced. If the frequency (f) is varied proportional to the information signal, *frequency shift keying* (FSK) is produced, and if the phase of the carrier (θ) is varied proportional to the information signal, *phase shift keying* (PSK) is produced. If both the amplitude and the phase are varied proportional to the information signal, *quadrature amplitude modulation* (QAM) results. ASK, FSK, PSK, and QAM are all forms of digital modulation:

$$v(t) = V \sin(2\pi \cdot ft + \boldsymbol{\theta}) \quad \begin{matrix} \text{ASK} & \text{FSK} & \text{PSK} \\ & \text{QAM} & \end{matrix} \tag{1}$$

Digital modulation is ideally suited to a multitude of communications applications, including both cable and wireless systems. Applications include the following: (1) relatively low-speed voice-band data communications modems, such as those found in most personal computers; (2) high-speed data transmission systems, such as broadband *digital subscriber lines* (DSL); (3) digital microwave and satellite communications systems; and (4) cellular telephone *Personal Communications Systems* (PCS).

Figure 1 shows a simplified block diagram for a digital modulation system. In the transmitter, the precoder performs level conversion and then encodes the incoming data into groups of bits that modulate an analog carrier. The modulated carrier is shaped (fil-

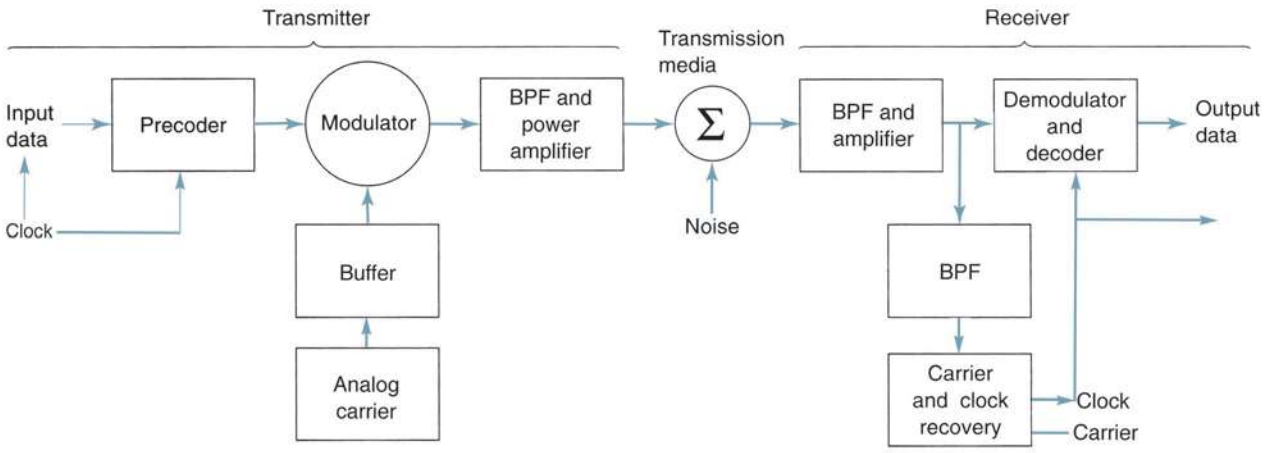


FIGURE 1 Simplified block diagram of a digital radio system

tered), amplified, and then transmitted through the transmission medium to the receiver. The transmission medium can be a metallic cable, optical fiber cable, Earth's atmosphere, or a combination of two or more types of transmission systems. In the receiver, the incoming signals are filtered, amplified, and then applied to the demodulator and decoder circuits, which extracts the original source information from the modulated carrier. The clock and carrier recovery circuits recover the analog carrier and digital timing (clock) signals from the incoming modulated wave since they are necessary to perform the demodulation process.

2 INFORMATION CAPACITY, BITS, BIT RATE, BAUD, AND *M*-ARY ENCODING

2-1 Information Capacity, Bits, and Bit Rate

Information theory is a highly theoretical study of the efficient use of bandwidth to propagate information through electronic communications systems. Information theory can be used to determine the *information capacity* of a data communications system. Information capacity is a measure of how much information can be propagated through a communications system and is a function of bandwidth and transmission time.

Information capacity represents the number of independent symbols that can be carried through a system in a given unit of time. The most basic digital symbol used to represent information is the *binary digit,* or *bit*. Therefore, it is often convenient to express the information capacity of a system as a *bit rate.* Bit rate is simply the number of bits transmitted during one second and is expressed in *bits per second* (bps).

In 1928, R. Hartley of Bell Telephone Laboratories developed a useful relationship among bandwidth, transmission time, and information capacity. Simply stated, Hartley's law is

$$I \propto B \times t \tag{2}$$

where I = information capacity (bits per second)
B = bandwidth (hertz)
t = transmission time (seconds)

From Equation 2, it can be seen that information capacity is a linear function of bandwidth and transmission time and is directly proportional to both. If either the bandwidth or the transmission time changes, a directly proportional change occurs in the information capacity.

In 1948, mathematician Claude E. Shannon (also of Bell Telephone Laboratories) published a paper in the *Bell System Technical Journal* relating the information capacity of a communications channel to bandwidth and *signal-to-noise ratio.* The higher the signal-to-noise ratio, the better the performance and the higher the information capacity. Mathematically stated, *the Shannon limit for information capacity* is

$$I = B \log_2\left(1 + \frac{S}{N}\right) \tag{3}$$

or

$$I = 3.32B \log_{10}\left(1 + \frac{S}{N}\right) \tag{4}$$

where I = information capacity (bps)
B = bandwidth (hertz)
$\frac{S}{N}$ = signal-to-noise power ratio (unitless)

For a standard telephone circuit with a signal-to-noise power ratio of 1000 (30 dB) and a bandwidth of 2.7 kHz, the Shannon limit for information capacity is

$$\begin{aligned} I &= (3.32)(2700) \log_{10} (1 + 1000) \\ &= 26.9 \text{ kbps} \end{aligned}$$

Shannon's formula is often misunderstood. The results of the preceding example indicate that 26.9 kbps can be propagated through a 2.7-kHz communications channel. This may be true, but it cannot be done with a binary system. To achieve an information transmission rate of 26.9 kbps through a 2.7-kHz channel, each symbol transmitted must contain more than one bit.

2-2 *M*-ary Encoding

M-ary is a term derived from the word *binary. M* simply represents a digit that corresponds to the number of conditions, levels, or combinations possible for a given number of binary variables. It is often advantageous to encode at a level higher than binary (sometimes referred to as *beyond binary* or *higher-than-binary encoding*) where there are more than two conditions possible. For example, a digital signal with four possible conditions (voltage levels, frequencies, phases, and so on) is an *M*-ary system where $M = 4$. If there are eight possible conditions, $M = 8$ and so forth. The number of bits necessary to produce a given number of conditions is expressed mathematically as

$$N = \log_2 M \tag{5}$$

where N = number of bits necessary
M = number of conditions, levels, or combinations possible with N bits

Equation 5 can be simplified and rearranged to express the number of conditions possible with N bits as

$$2^N = M \tag{6}$$

For example, with one bit, only $2^1 = 2$ conditions are possible. With two bits, $2^2 = 4$ conditions are possible, with three bits, $2^3 = 8$ conditions are possible, and so on.

2-3 Baud and Minimum Bandwidth

Baud is a term that is often misunderstood and commonly confused with bit rate (bps). Bit rate refers to the rate of change of a digital information signal, which is usually binary. Baud, like bit rate, is also a rate of change; however, baud refers to the rate of change of a signal on the transmission medium after encoding and modulation have occurred. Hence, baud is a unit of transmission rate, modulation rate, or symbol rate and, therefore, the terms *symbols per second* and *baud* are often used interchangeably. Mathematically, baud is the reciprocal of the time of one output *signaling element,* and a signaling element may represent several information bits. Baud is expressed as

$$\text{baud} = \frac{1}{t_s} \tag{7}$$

where baud = symbol rate (baud per second)
t_s = time of one signaling element (seconds)

A signaling element is sometimes called a *symbol* and could be encoded as a change in the amplitude, frequency, or phase. For example, binary signals are generally encoded and transmitted one bit at a time in the form of discrete voltage levels representing logic 1s (highs) and logic 0s (lows). A baud is also transmitted one at a time; however, a baud may represent more than one information bit. Thus, the baud of a data communications system may be considerably less than the bit rate. In binary systems (such as binary FSK and binary PSK), *baud* and *bits per second* are equal. However, in higher-level systems (such as QPSK and 8-PSK), bps is always greater than baud.

According to H. Nyquist, binary digital signals can be propagated through an ideal noiseless transmission medium at a rate equal to two times the bandwidth of the medium. The minimum theoretical bandwidth necessary to propagate a signal is called the minimum *Nyquist bandwidth* or sometimes the minimum *Nyquist frequency.* Thus, $f_b = 2B$, where f_b is the bit rate in bps and B is the *ideal Nyquist bandwidth.* The actual bandwidth necessary to propagate a given bit rate depends on several factors, including the type of encoding and modulation used, the types of filters used, system noise, and desired error performance. The ideal bandwidth is generally used for comparison purposes only.

The relationship between bandwidth and bit rate also applies to the opposite situation. For a given bandwidth (B), the highest theoretical bit rate is $2B$. For example, a standard telephone circuit has a bandwidth of approximately 2700 Hz, which has the capacity to propagate 5400 bps through it. However, if more than two levels are used for signaling (higher-than-binary encoding), more than one bit may be transmitted at a time, and it is possible to propagate a bit rate that exceeds $2B$. Using multilevel signaling, the Nyquist formulation for channel capacity is

$$f_b = 2B \log_2 M \tag{8}$$

where f_b = channel capacity (bps)
B = minimum Nyquist bandwidth (hertz)
M = number of discrete signal or voltage levels

Equation 8 can be rearranged to solve for the minimum bandwidth necessary to pass M-ary digitally modulated carriers

$$B = \left(\frac{f_b}{\log_2 M}\right) \tag{9}$$

If N is substituted for $\log_2 M$, Equation 9 reduces to

$$B = \frac{f_b}{N} \tag{10}$$

where N is the number of bits encoded into each signaling element.

If information bits are encoded (grouped) and then converted to signals with more than two levels, transmission rates in excess of $2B$ are possible, as will be seen in subsequent sections of this chapter. In addition, since baud is the encoded rate of change, it also equals the bit rate divided by the number of bits encoded into one signaling element. Thus,

$$\text{baud} = \frac{f_b}{N} \tag{11}$$

By comparing Equation 10 with Equation 11, it can be seen that with digital modulation, the baud and the ideal minimum Nyquist bandwidth have the same value and are equal to the bit rate divided by the number of bits encoded. This statement holds true for all forms of digital modulation except frequency-shift keying.

3 AMPLITUDE-SHIFT KEYING

The simplest digital modulation technique is *amplitude-shift keying* (ASK), where a binary information signal directly modulates the amplitude of an analog carrier. ASK is similar to standard amplitude modulation except there are only two output amplitudes possible. Amplitude-shift keying is sometimes called *digital amplitude modulation* (DAM). Mathematically, amplitude-shift keying is

$$v_{(ask)}(t) = [1 + v_m(t)]\left[\frac{A}{2}\cos(\omega_c t)\right] \tag{12}$$

where $v_{ask}(t)$ = amplitude-shift keying wave
$v_m(t)$ = digital information (modulating) signal (volts)
$A/2$ = unmodulated carrier amplitude (volts)
ω_c = analog carrier radian frequency (radians per second, $2\pi f_c t$)

In Equation 12, the modulating signal ($v_m[t]$) is a normalized binary waveform, where +1 V = logic 1 and −1 V = logic 0. Therefore, for a logic 1 input, $v_m(t) = +1$ V, Equation 12 reduces to

$$\begin{aligned} v_{(ask)}(t) &= [1 + 1]\left[\frac{A}{2}\cos(\omega_c t)\right] \\ &= A\cos(\omega_c t) \end{aligned}$$

and for a logic 0 input, $v_m(t) = -1$ V, Equation 12 reduces to

$$\begin{aligned} v_{(ask)}(t) &= [1 - 1]\left[\frac{A}{2}\cos(\omega_c t)\right] \\ &= 0 \end{aligned}$$

Thus, the modulated wave $v_{ask}(t)$, is either $A\cos(\omega_c t)$ or 0. Hence, the carrier is either "*on*" or "*off*," which is why amplitude-shift keying is sometimes referred to as *on-off keying* (OOK).

Figure 2 shows the input and output waveforms from an ASK modulator. From the figure, it can be seen that for every change in the input binary data stream, there is one change in the ASK waveform, and the time of one bit (t_b) equals the time of one analog signaling element (t_s). It is also important to note that for the entire time the binary input is high, the output is a constant-amplitude, constant-frequency signal, and for the entire time the binary input is low, the carrier is off. The bit time is the reciprocal of the bit rate and the time of one signaling element is the reciprocal of the baud. Therefore, the rate of change of the

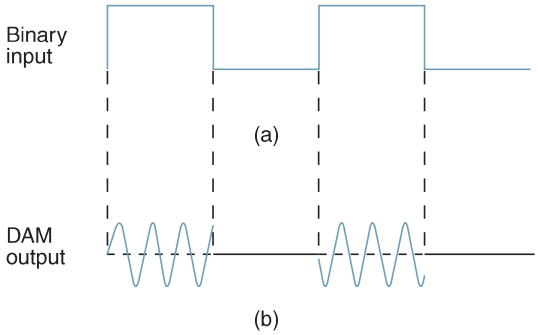


FIGURE 2 Digital amplitude modulation: (a) input binary; (b) output DAM waveform

ASK waveform (baud) is the same as the rate of change of the binary input (bps); thus, the bit rate equals the baud. With ASK, the bit rate is also equal to the minimum Nyquist bandwidth. This can be verified by substituting into Equations 10 and 11 and setting N to 1:

$$B = \frac{f_b}{1} = f_b \qquad \text{baud} = \frac{f_b}{1} = f_b$$

Example 1

Determine the baud and minimum bandwidth necessary to pass a 10 kbps binary signal using amplitude shift keying.

Solution For ASK, $N = 1$, and the baud and minimum bandwidth are determined from Equations 11 and 10, respectively:

$$B = \frac{10{,}000}{1} = 10{,}000$$

$$\text{baud} = \frac{10{,}000}{1} = 10{,}000$$

The use of amplitude-modulated analog carriers to transport digital information is a relatively low-quality, low-cost type of digital modulation and, therefore, is seldom used except for very low-speed telemetry circuits.

4 FREQUENCY-SHIFT KEYING

Frequency-shift keying (FSK) is another relatively simple, low-performance type of digital modulation. FSK is a form of constant-amplitude angle modulation similar to standard frequency modulation (FM) except the modulating signal is a binary signal that varies between two discrete voltage levels rather than a continuously changing analog waveform. Consequently, FSK is sometimes called *binary FSK* (BFSK). The general expression for FSK is

$$v_{fsk}(t) = V_c \cos\{2\pi[f_c + v_m(t)\,\Delta f]t\} \tag{13}$$

where $v_{fsk}(t)$ = binary FSK waveform
V_c = peak analog carrier amplitude (volts)
f_c = analog carrier center frequency (hertz)
Δf = peak change (shift) in the analog carrier frequency (hertz)
$v_m(t)$ = binary input (modulating) signal (volts)

From Equation 13, it can be seen that the peak shift in the carrier frequency (Δf) is proportional to the amplitude of the binary input signal ($v_m[t]$), and the direction of the shift

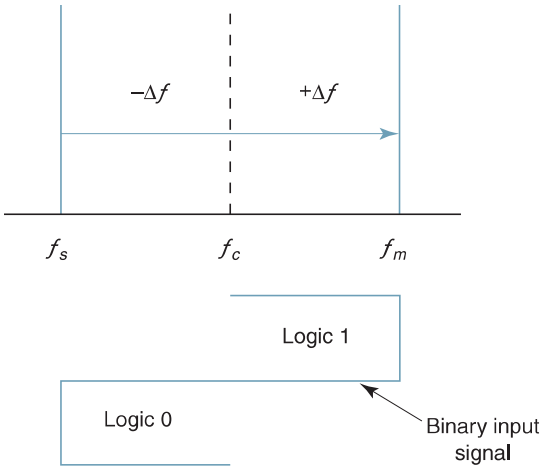


FIGURE 3 FSK in the frequency domain

is determined by the polarity. The modulating signal is a normalized binary waveform where a logic 1 = +1 V and a logic 0 = −1 V. Thus, for a logic 1 input, $v_m(t) = +1$, Equation 13 can be rewritten as

$$v_{fsk}(t) = V_c \cos[2\pi(f_c + \Delta f)t]$$

For a logic 0 input, $v_m(t) = -1$, Equation 13 becomes

$$v_{fsk}(t) = V_c \cos[2\pi(f_c - \Delta f)t]$$

With binary FSK, the carrier center frequency (f_c) is shifted (deviated) up and down in the frequency domain by the binary input signal as shown in Figure 3. As the binary input signal changes from a logic 0 to a logic 1 and vice versa, the output frequency shifts between two frequencies: a mark, or logic 1 frequency (f_m), and a space, or logic 0 frequency (f_s). The mark and space frequencies are separated from the carrier frequency by the peak frequency deviation (Δf) and from each other by 2 Δf.

With FSK, frequency deviation is defined as the difference between either the mark or space frequency and the center frequency, or half the difference between the mark and space frequencies. Frequency deviation is illustrated in Figure 3 and expressed mathematically as

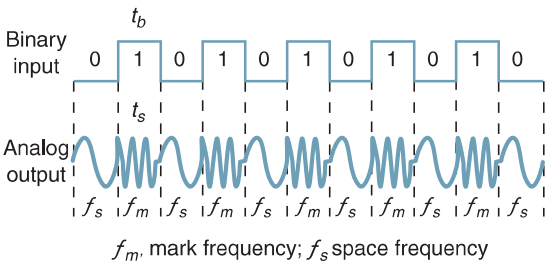
$$\Delta f = \frac{|f_m - f_s|}{2} \tag{14}$$

where Δf = frequency deviation (hertz)
$|f_m - f_s|$ = absolute difference between the mark and space frequencies (hertz)

Figure 4a shows in the time domain the binary input to an FSK modulator and the corresponding FSK output. As the figure shows, when the binary input (f_b) changes from a logic 1 to a logic 0 and vice versa, the FSK output frequency shifts from a mark (f_m) to a space (f_s) frequency and vice versa. In Figure 4a, the mark frequency is the higher frequency ($f_c + \Delta f$), and the space frequency is the lower frequency ($f_c - \Delta f$), although this relationship could be just the opposite. Figure 4b shows the truth table for a binary FSK modulator. The truth table shows the input and output possibilities for a given digital modulation scheme.

4-1 FSK Bit Rate, Baud, and Bandwidth

In Figure 4a, it can be seen that the time of one bit (t_b) is the same as the time the FSK output is a mark of space frequency (t_s). Thus, the bit time equals the time of an FSK signaling element, and the bit rate equals the baud.



(a)

binary input	frequency output
0	space (f_s)
1	mark (f_m)

(b)

FIGURE 4 FSK in the time domain: (a) waveform; (b) truth table

The baud for binary FSK can also be determined by substituting $N = 1$ in Equation 11:

$$\text{baud} = \frac{f_b}{1} = f_b$$

FSK is the exception to the rule for digital modulation, as the minimum bandwidth is not determined from Equation 10. The minimum bandwidth for FSK is given as

$$\begin{aligned} B &= |(f_s - f_b) - (f_m - f_b)| \\ &= |f_s - f_m| + 2f_b \end{aligned}$$

and since $|f_s - f_m|$ equals $2\Delta f$, the minimum bandwidth can be approximated as

$$B = 2(\Delta f + f_b) \tag{15}$$

where B = minimum Nyquist bandwidth (hertz)
Δf = frequency deviation ($|f_m - f_s|$) (hertz)
f_b = input bit rate (bps)

Note how closely Equation 15 resembles Carson's rule for determining the approximate bandwidth for an FM wave. The only difference in the two equations is that, for FSK, the bit rate (f_b) is substituted for the modulating-signal frequency (f_m).

Example 2

Determine (a) the peak frequency deviation, (b) minimum bandwidth, and (c) baud for a binary FSK signal with a mark frequency of 49 kHz, a space frequency of 51 kHz, and an input bit rate of 2 kbps.

Solution **a.** The peak frequency deviation is determined from Equation 14:

$$\Delta f = \frac{|49\text{kHz} - 51\text{kHz}|}{2}$$

$$= 1 \text{ kHz}$$

b. The minimum bandwidth is determined from Equation 15:

$$B = 2(1000 + 2000)$$

$$= 6 \text{ kHz}$$

c. For FSK, $N = 1$, and the baud is determined from Equation 11 as

$$\text{baud} = \frac{2000}{1} = 2000$$

Bessel functions can also be used to determine the approximate bandwidth for an FSK wave. As shown in Figure 5, the fastest rate of change (highest fundamental frequency) in a nonreturn-to-zero (NRZ) binary signal occurs when alternating 1s and 0s are occurring (i.e., a square wave). Since it takes a high and a low to produce a cycle, the highest fundamental frequency present in a square wave equals the repetition rate of the square wave, which with a binary signal is equal to half the bit rate. Therefore,

$$f_a = \frac{f_b}{2} \tag{16}$$

where f_a = highest fundamental frequency of the binary input signal (hertz)
f_b = input bit rate (bps)

The formula used for modulation index in FM is also valid for FSK; thus,

$$h = \frac{\Delta f}{f_a} \qquad \text{(unitless)} \tag{17}$$

where h = FM modulation index called the h-factor in FSK
f_a = fundamental frequency of the binary modulating signal (hertz)
Δf = peak frequency deviation (hertz)

The worst-case modulation index (deviation ratio) is that which yields the widest bandwidth. The worst-case or widest bandwidth occurs when both the frequency deviation and the modulating-signal frequency are at their maximum values. As described earlier, the peak frequency deviation in FSK is constant and always at its maximum value, and the highest fundamental frequency is equal to half the incoming bit rate. Thus,

$$h = \frac{\dfrac{|f_m - f_s|}{2}}{\dfrac{f_b}{2}} \qquad \text{(unitless)}$$

or

$$h = \frac{|f_m - f_s|}{f_b} \tag{18}$$

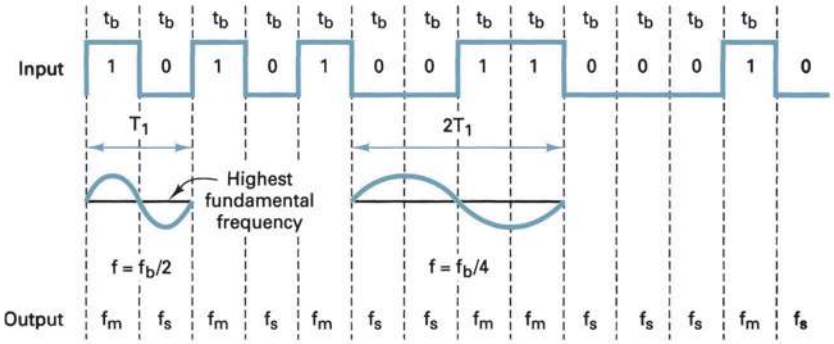


FIGURE 5 FSK modulator, t_b, time of one bit = $1/f_b$; f_m, mark frequency; f_s, space frequency; T_1, period of shortest cycle; $1/T_1$, fundamental frequency of binary square wave; f_b, input bit rate (bps)

where h = h-factor (unitless)
f_m = mark frequency (hertz)
f_s = space frequency (hertz)
f_b = bit rate (bits per second)

Example 3

Using a Bessel table, determine the minimum bandwidth for the same FSK signal described in Example 1 with a mark frequency of 49 kHz, a space frequency of 51 kHz, and an input bit rate of 2 kbps.

Solution The modulation index is found by substituting into Equation 17:

$$h = \frac{|49 \text{ kHz} - 51 \text{ kHz}|}{2 \text{ kbps}}$$

or

$$= \frac{2 \text{ kHz}}{2 \text{ kbps}}$$

$$= 1$$

From a Bessel table, three sets of significant sidebands are produced for a modulation index of one. Therefore, the bandwidth can be determined as follows:

$$B = 2(3 \times 1000)$$

$$= 6000 \text{ Hz}$$

The bandwidth determined in Example 3 using the Bessel table is identical to the bandwidth determined in Example 2.

4-2 FSK Transmitter

Figure 6 shows a simplified binary FSK modulator, which is very similar to a conventional FM modulator and is very often a voltage-controlled oscillator (VCO). The center frequency (f_c) is chosen such that it falls halfway between the mark and space frequencies. A logic 1 input shifts the VCO output to the mark frequency, and a logic 0 input shifts the VCO output to the space frequency. Consequently, as the binary input signal changes back and forth between logic 1 and logic 0 conditions, the VCO output shifts or deviates back and forth between the mark and space frequencies.

In a binary FSK modulator, Δf is the peak frequency deviation of the carrier and is equal to the difference between the carrier rest frequency and either the mark or the space frequency (or half the difference between the carrier rest frequency) and either the mark or the space frequency (or half the difference between the mark and space frequencies). A VCO-FSK modulator can be operated in the sweep mode where the peak frequency deviation is

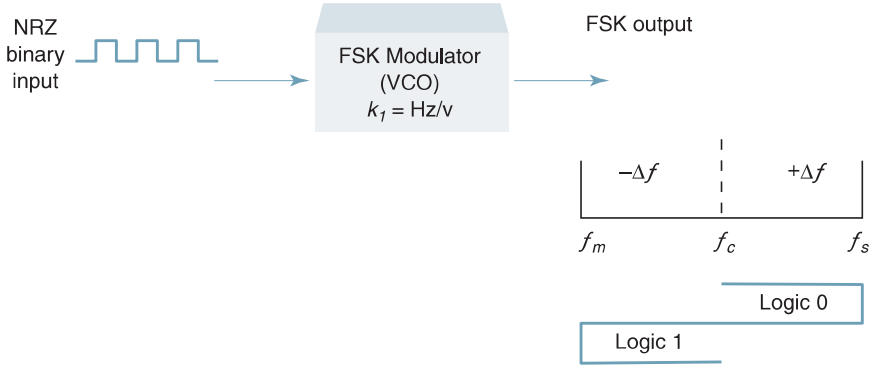


FIGURE 6 FSK modulator

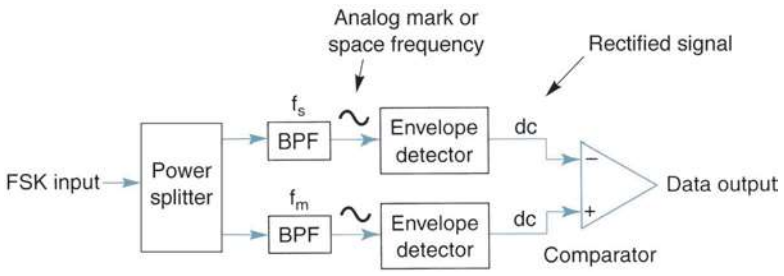


FIGURE 7 Noncoherent FSK demodulator

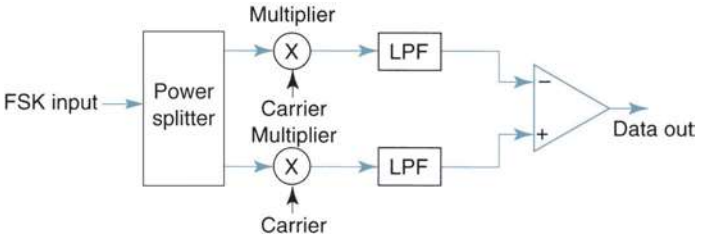


FIGURE 8 Coherent FSK demodulator

simply the product of the binary input voltage and the deviation sensitivity of the VCO. With the sweep mode of modulation, the frequency deviation is expressed mathematically as

$$\Delta f = v_m(t)k_l \tag{19}$$

where Δf = peak frequency deviation (hertz)
$v_m(t)$ = peak binary modulating-signal voltage (volts)
k_l = deviation sensitivity (hertz per volt).

With binary FSK, the amplitude of the input signal can only be one of two values, one for a logic 1 condition and one for a logic 0 condition. Therefore, the peak frequency deviation is constant and always at its maximum value. Frequency deviation is simply plus or minus the peak voltage of the binary signal times the deviation sensitivity of the VCO. Since the peak voltage is the same for a logic 1 as it is for a logic 0, the magnitude of the frequency deviation is also the same for a logic 1 as it is for a logic 0.

4-3 FSK Receiver

FSK demodulation is quite simple with a circuit such as the one shown in Figure 7. The FSK input signal is simultaneously applied to the inputs of both bandpass filters (BPFs) through a power splitter. The respective filter passes only the mark or only the space frequency on to its respective envelope detector. The envelope detectors, in turn, indicate the total power in each passband, and the comparator responds to the largest of the two powers. This type of FSK detection is referred to as noncoherent detection; there is no frequency involved in the demodulation process that is synchronized either in phase, frequency, or both with the incoming FSK signal.

Figure 8 shows the block diagram for a coherent FSK receiver. The incoming FSK signal is multiplied by a recovered carrier signal that has the exact same frequency and phase as the transmitter reference. However, the two transmitted frequencies (the mark and space frequencies) are not generally continuous; it is not practical to reproduce a local reference that is coherent with both of them. Consequently, coherent FSK detection is seldom used.

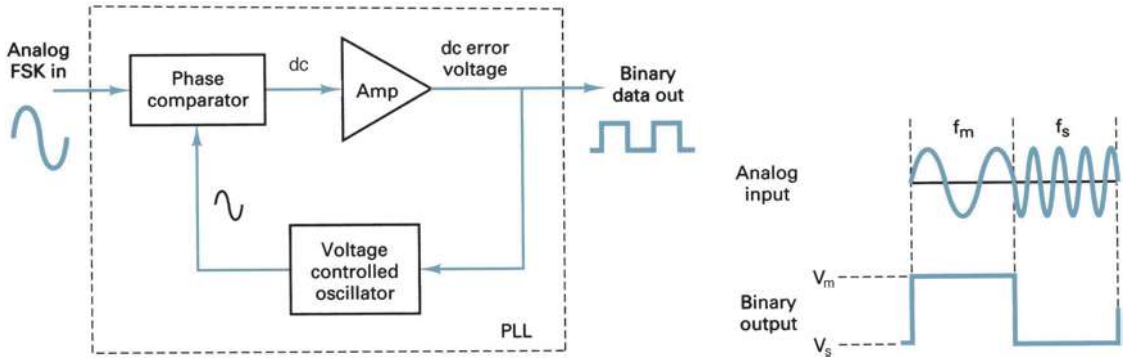


FIGURE 9 PLL-FSK demodulator

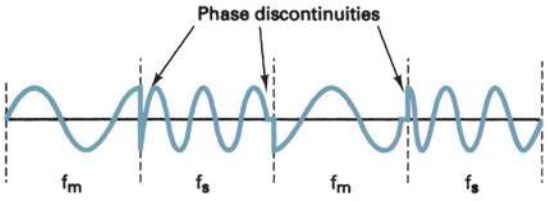


FIGURE 10 Noncontinuous FSK waveform

The most common circuit used for demodulating binary FSK signals is the *phase-locked loop* (PLL), which is shown in block diagram form in Figure 9. A PLL-FSK demodulator works similarly to a PLL-FM demodulator. As the input to the PLL shifts between the mark and space frequencies, the *dc error voltage* at the output of the phase comparator follows the frequency shift. Because there are only two input frequencies (mark and space), there are also only two output error voltages. One represents a logic 1 and the other a logic 0. Therefore, the output is a two-level (binary) representation of the FSK input. Generally, the natural frequency of the PLL is made equal to the center frequency of the FSK modulator. As a result, the changes in the dc error voltage follow the changes in the analog input frequency and are symmetrical around 0 V.

Binary FSK has a poorer error performance than PSK or QAM and, consequently, is seldom used for high-performance digital radio systems. Its use is restricted to low-performance, low-cost, asynchronous data modems that are used for data communications over analog, voice-band telephone lines.

4-4 Continuous-Phase Frequency-Shift Keying

Continuous-phase frequency-shift keying (CP-FSK) is binary FSK except the mark and space frequencies are synchronized with the input binary bit rate. Synchronous simply implies that there is a precise time relationship between the two; it does not mean they are equal. With CP-FSK, the mark and space frequencies are selected such that they are separated from the center frequency by an exact multiple of one-half the bit rate (f_m and $f_s = n[f_b/2]$), where n = any integer). This ensures a smooth phase transition in the analog output signal when it changes from a mark to a space frequency or vice versa. Figure 10 shows a noncontinuous FSK waveform. It can be seen that when the input changes from a logic 1 to a logic 0 and vice versa, there is an abrupt phase discontinuity in the analog signal. When this occurs, the demodulator has trouble following the frequency shift; consequently, an error may occur.

Figure 11 shows a continuous phase FSK waveform. Notice that when the output frequency changes, it is a smooth, continuous transition. Consequently, there are no phase discontinuities. CP-FSK has a better bit-error performance than conventional binary FSK for a given signal-to-noise ratio. The disadvantage of CP-FSK is that it requires synchronization circuits and is, therefore, more expensive to implement.

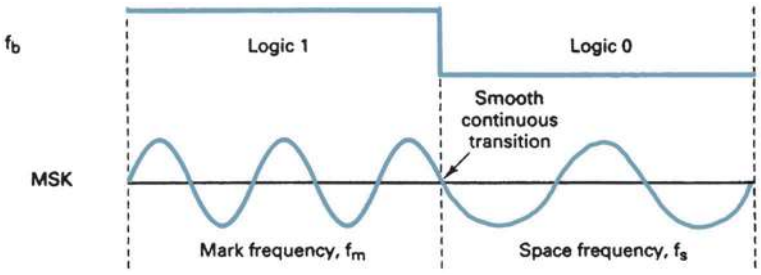


FIGURE 11 Continuous-phase MSK waveform

5 PHASE-SHIFT KEYING

Phase-shift keying (PSK) is another form of *angle-modulated, constant-amplitude* digital modulation. PSK is an *M*-ary digital modulation scheme similar to conventional phase modulation except with PSK the input is a binary digital signal and there are a limited number of output phases possible. The input binary information is encoded into groups of bits before modulating the carrier. The number of bits in a group ranges from 1 to 12 or more. The number of output phases is defined by *M* as described in Equation 6 and determined by the number of bits in the group (*n*).

5-1 Binary Phase-Shift Keying

The simplest form of PSK is *binary phase-shift keying* (BPSK), where $N = 1$ and $M = 2$. Therefore, with BPSK, two phases ($2^1 = 2$) are possible for the carrier. One phase represents a logic 1, and the other phase represents a logic 0. As the input digital signal changes state (i.e., from a 1 to a 0 or from a 0 to a 1), the phase of the output carrier shifts between two angles that are separated by 180°. Hence, other names for BPSK are *phase reversal keying* (PRK) and *biphase modulation*. BPSK is a form of square-wave modulation of a *continuous wave* (CW) signal.

5-1-1 BPSK transmitter. Figure 12 shows a simplified block diagram of a BPSK transmitter. The balanced modulator acts as a phase reversing switch. Depending on the

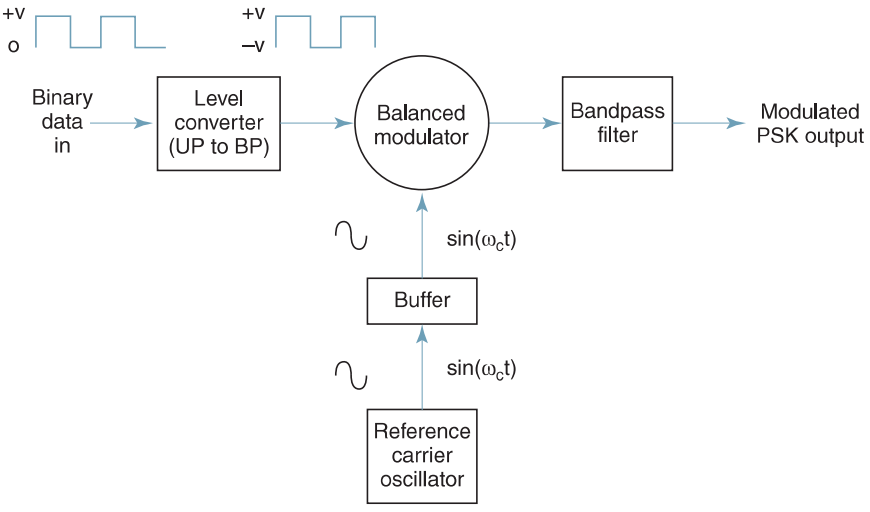


FIGURE 12 BPSK transmitter

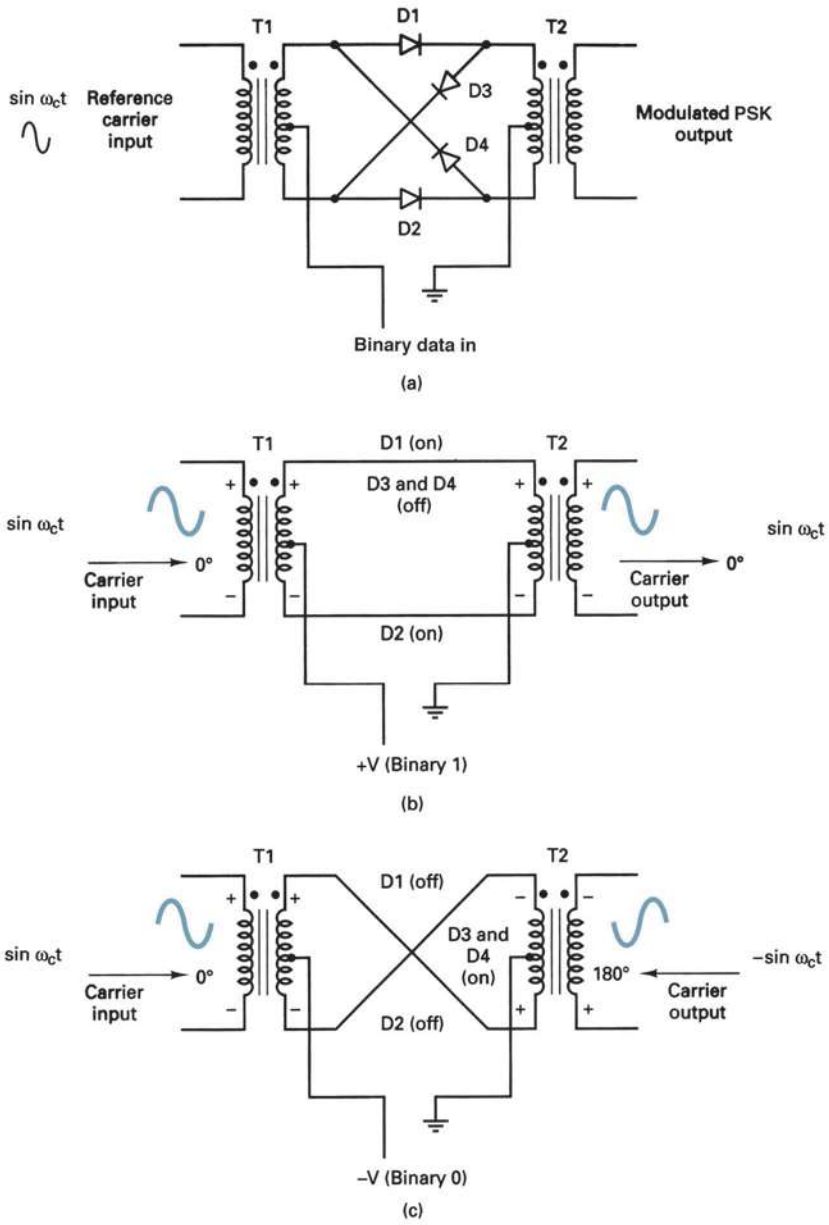


FIGURE 13 (a) Balanced ring modulator; (b) logic 1 input; (c) logic 0 input

logic condition of the digital input, the carrier is transferred to the output either in phase or 180° out of phase with the reference carrier oscillator.

Figure 13 shows the schematic diagram of a balanced ring modulator. The balanced modulator has two inputs: a carrier that is in phase with the reference oscillator and the binary digital data. For the balanced modulator to operate properly, the digital input voltage must be much greater than the peak carrier voltage. This ensures that the digital input controls the on/off state of diodes D1 to D4. If the binary input is a logic 1 (positive voltage), diodes D1 and D2 are forward biased and on, while diodes D3 and D4 are reverse biased and off (Figure 13b). With the polarities shown, the carrier voltage is developed across

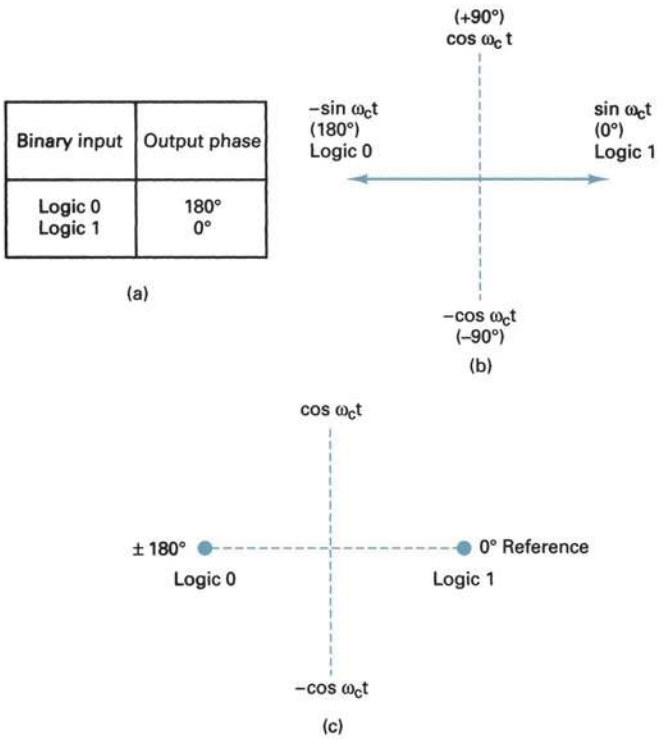


FIGURE 14 BPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

transformer T2 in phase with the carrier voltage across T1. Consequently, the output signal is in phase with the reference oscillator.

If the binary input is a logic 0 (negative voltage), diodes D1 and D2 are reverse biased and off, while diodes D3 and D4 are forward biased and on (Figure 13c). As a result, the carrier voltage is developed across transformer T2 180° out of phase with the carrier voltage across T1. Consequently, the output signal is 180° out of phase with the reference oscillator. Figure 14 shows the truth table, phasor diagram, and constellation diagram for a BPSK modulator. A *constellation diagram,* which is sometimes called a *signal state-space diagram,* is similar to a phasor diagram except that the entire phasor is not drawn. In a constellation diagram, only the relative positions of the peaks of the phasors are shown.

5-1-2 Bandwidth considerations of BPSK. A balanced modulator is a *product modulator;* the output signal is the product of the two input signals. In a BPSK modulator, the carrier input signal is multiplied by the binary data. If +1 V is assigned to a logic 1 and −1 V is assigned to a logic 0, the input carrier ($\sin \omega_c t$) is multiplied by either a + or −1. Consequently, the output signal is either $+1 \sin \omega_c t$ or $-1 \sin \omega_c t$; the first represents a signal that is *in phase* with the reference oscillator, the latter a signal that is 180° out of phase with the reference oscillator. Each time the input logic condition changes, the output phase changes. Consequently, for BPSK, the output rate of change (baud) is equal to the input rate of change (bps), and the widest output bandwidth occurs when the input binary data are an alternating 1/0 sequence. The fundamental frequency (f_a) of an alternative 1/0 bit sequence is equal to one-half of the bit rate ($f_b/2$). Mathematically, the output of a BPSK modulator is proportional to

$$\text{BPSK output} = [\sin(2\pi f_a t)] \times [\sin(2\pi f_c t)] \tag{20}$$

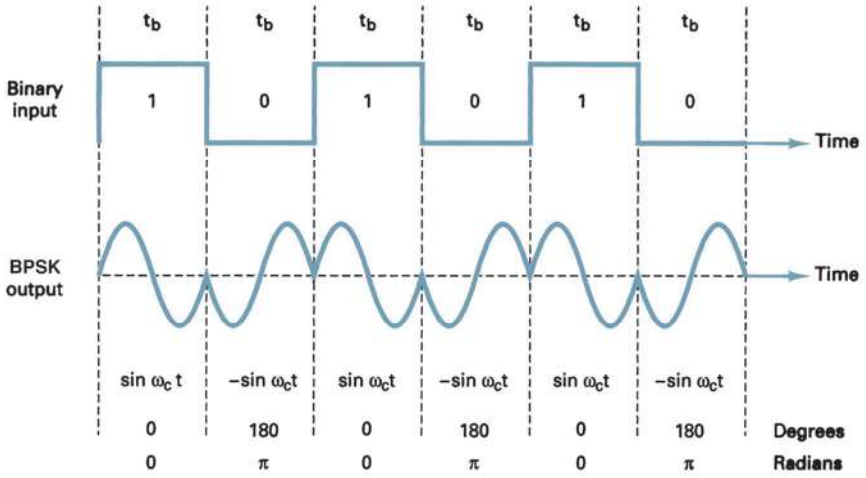


FIGURE 15 Output phase-versus-time relationship for a BPSK modulator

where f_a = maximum fundamental frequency of binary input (hertz)
f_c = reference carrier frequency (hertz)

Solving for the trig identity for the product of two sine functions,

$$\frac{1}{2}\cos[2\pi(f_c - f_a)t] - \frac{1}{2}\cos[2\pi(f_c + f_a)t]$$

Thus, the minimum double-sided Nyquist bandwidth (B) is

$$\begin{array}{r} f_c + f_a \\ \underline{-(f_c + f_a)} \end{array} \quad \text{or} \quad \frac{f_c + f_a}{\underline{-f_c + f_a}} \\ 2f_a$$

and because $f_a = f_b/2$, where f_b = input bit rate,

$$B = \frac{2f_b}{2} = f_b$$

where B is the minimum double-sided Nyquist bandwidth.

Figure 15 shows the output phase-versus-time relationship for a BPSK waveform. As the figure shows, a logic 1 input produces an analog output signal with a 0° phase angle, and a logic 0 input produces an analog output signal with a 180° phase angle. As the binary input shifts between a logic 1 and a logic 0 condition and vice versa, the phase of the BPSK waveform shifts between 0° and 180°, respectively. For simplicity, only one cycle of the analog carrier is shown in each signaling element, although there may be anywhere between a fraction of a cycle to several thousand cycles, depending on the relationship between the input bit rate and the analog carrier frequency. It can also be seen that the time of one BPSK signaling element (t_s) is equal to the time of one information bit (t_b), which indicates that the bit rate equals the baud.

Example 4

For a BPSK modulator with a carrier frequency of 70 MHz and an input bit rate of 10 Mbps, determine the maximum and minimum upper and lower side frequencies, draw the output spectrum, determine the minimum Nyquist bandwidth, and calculate the baud.

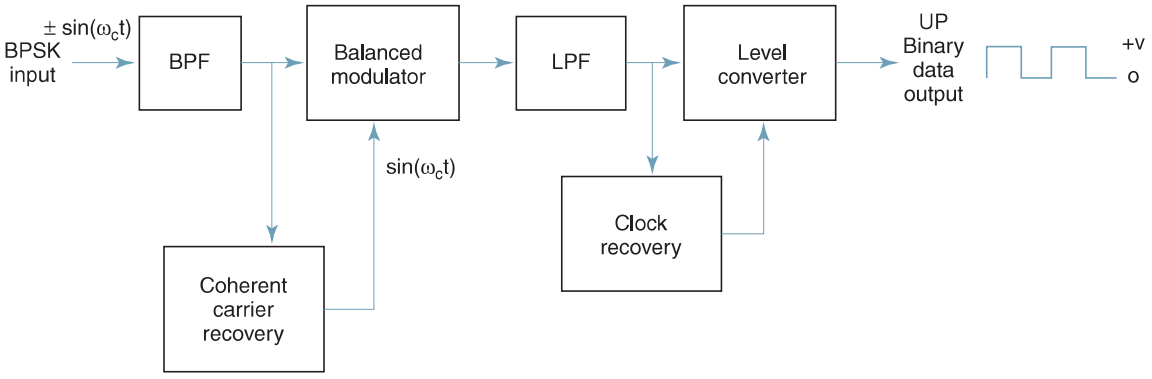


FIGURE 16 Block diagram of a BPSK receiver

Solution Substituting into Equation 20 yields

$$\text{output} = (\sin \omega_a t)(\sin \omega_c t)$$
$$= [\sin 2\pi(5 \text{ MHz})t][\sin 2\pi(70 \text{ MHz})t]$$
$$= \underbrace{\frac{1}{2}\cos 2\pi(70 \text{ MHz} - 5 \text{ MHz})t}_{\text{lower side frequency}} - \underbrace{\frac{1}{2}\cos 2\pi(70 \text{ MHz} + 5 \text{ MHz})t}_{\text{upper side frequency}}$$

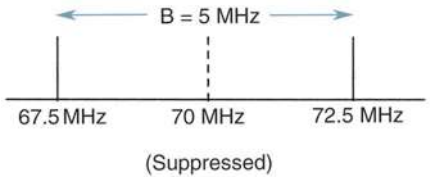
Minimum lower side frequency (LSF):

$$\text{LSF} = 70 \text{ MHz} - 5 \text{ MHz} = 65 \text{ MHz}$$

Maximum upper side frequency (USF):

$$\text{USF} = 70 \text{ MHz} + 5 \text{ MHz} = 75 \text{ MHz}$$

Therefore, the output spectrum for the worst-case binary input conditions is as follows:
The minimum Nyquist bandwidth (B) is



$$B = 75 \text{ MHz} - 65 \text{ MHz} = 10 \text{ MHz}$$

and the baud $= f_b$, or 10 megabaud.

5-1-3 BPSK receiver. Figure 16 shows the block diagram of a BPSK receiver. The input signal may be $+\sin \omega_c t$ or $-\sin \omega_c t$. The coherent carrier recovery circuit detects and regenerates a carrier signal that is both frequency and phase coherent with the original transmit carrier. The balanced modulator is a product detector; the output is the product of the two inputs (the BPSK signal and the recovered carrier). The low-pass filter (LPF) separates the recovered binary data from the complex demodulated signal. Mathematically, the demodulation process is as follows.

For a BPSK input signal of $+\sin \omega_c t$ (logic 1), the output of the balanced modulator is

$$\text{output} = (\sin \omega_c t)(\sin \omega_c t) = \sin^2 \omega_c t \quad (21)$$

$$\text{or} \qquad \sin^2 \omega_c t = \frac{1}{2}(1 - \cos 2\omega_c t) = \frac{1}{2} - \frac{1}{2}\cos 2\,\omega_c t \quad \text{(filtered out)}$$

$$\text{leaving} \qquad \text{output} = +\frac{1}{2}\text{V} = \text{logic 1}$$

It can be seen that the output of the balanced modulator contains a positive voltage (+[1/2]V) and a cosine wave at twice the carrier frequency (2 ω_c) The LPF has a cutoff frequency much lower than $2\omega_c$ and, thus, blocks the second harmonic of the carrier and passes only the positive constant component. A positive voltage represents a demodulated logic 1.

For a BPSK input signal of $-\sin \omega_c t$ (logic 0), the output of the balanced modulator is

$$\text{output} = (-\sin \omega_c t)(\sin \omega_c t) = -\sin^2 \omega_c t$$

$$\text{or} \qquad -\sin^2 \omega_c t = -\frac{1}{2}(1 - \cos 2\omega_c t) = -\frac{1}{2} + \frac{1}{2}\cos 2\omega_c t \quad \text{(filtered out)}$$

$$\text{leaving} \qquad \text{output} = -\frac{1}{2}\text{V} = \text{logic 0}$$

The output of the balanced modulator contains a negative voltage (−[1/2]V) and a cosine wave at twice the carrier frequency ($2\omega_c$). Again, the LPF blocks the second harmonic of the carrier and passes only the negative constant component. A negative voltage represents a demodulated logic 0.

5-2 Quaternary Phase-Shift Keying

Quaternary phase shift keying (QPSK), or *quadrature* PSK as it is sometimes called, is another form of angle-modulated, constant-amplitude digital modulation. QPSK is an *M*-ary encoding scheme where $N = 2$ and $M = 4$ (hence, the name "quaternary" meaning "4"). With QPSK, four output phases are possible for a single carrier frequency. Because there are four output phases, there must be four different input conditions. Because the digital input to a QPSK modulator is a binary (base 2) signal, to produce four different input combinations, the modulator requires more than a single input bit to determine the output condition. With two bits, there are four possible conditions: 00, 01, 10, and 11. Therefore, with QPSK, the binary input data are combined into groups of two bits, called *dibits*. In the modulator, each dibit code generates one of the four possible output phases (+45°, +135°, −45°, and −135°). Therefore, for each two-bit dibit clocked into the modulator, a single output change occurs, and the rate of change at the output (baud) is equal to one-half the input bit rate (i.e., two input bits produce one output phase change).

5-2-1 QPSK transmitter. A block diagram of a QPSK modulator is shown in Figure 17. Two bits (a dibit) are clocked into the bit splitter. After both bits have been serially inputted, they are simultaneously parallel outputted. One bit is directed to the I channel and the other to the Q channel. The I bit modulates a carrier that is in phase with the reference oscillator (hence the name "I" for "in phase" channel), and the Q bit modulates a carrier that is 90° out of phase or in quadrature with the reference carrier (hence the name "Q" for "quadrature" channel).

It can be seen that once a dibit has been split into the I and Q channels, the operation is the same as in a BPSK modulator. Essentially, a QPSK modulator is two BPSK modulators combined in parallel. Again, for a logic 1 = +1 V and a logic 0 = −1 V, two phases are possible at the output of the I balanced modulator ($+\sin \omega_c t$ and $-\sin \omega_c t$), and two

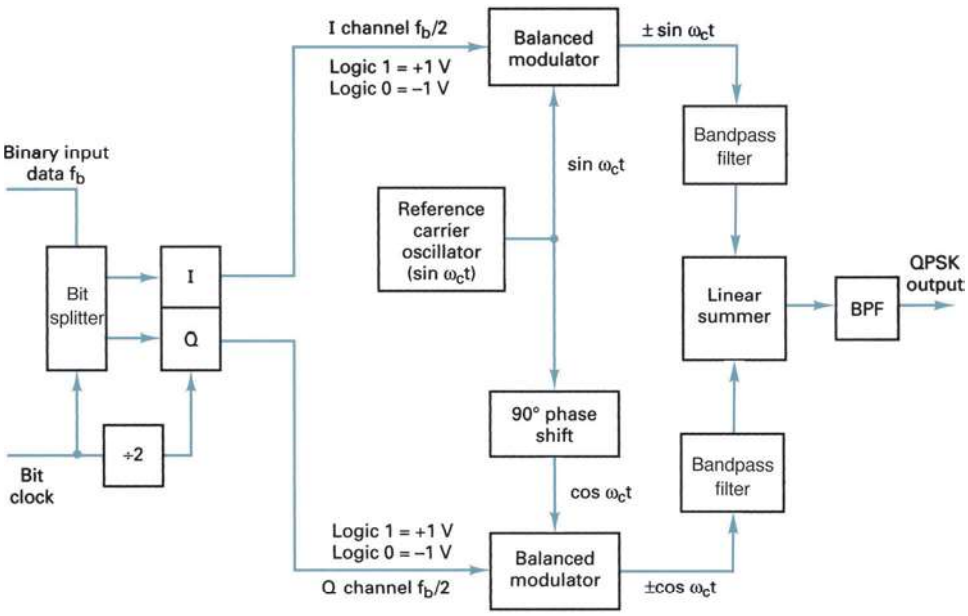


FIGURE 17 QPSK modulator

phases are possible at the output of the Q balanced modulator ($+\cos \omega_c t$ and $-\cos \omega_c t$). When the linear summer combines the two quadrature (90° out of phase) signals, there are four possible resultant phasors given by these expressions: $+ \sin \omega_c t + \cos \omega_c t$, $+ \sin \omega_c t - \cos \omega_c t$, $-\sin \omega_c t + \cos \omega_c t$, and $-\sin \omega_c t - \cos \omega_c t$.

Example 5

For the QPSK modulator shown in Figure 17, construct the truth table, phasor diagram, and constellation diagram.

Solution For a binary data input of Q = 0 and I = 0, the two inputs to the I balanced modulator are -1 and $\sin \omega_c t$, and the two inputs to the Q balanced modulator are -1 and $\cos \omega_c t$. Consequently, the outputs are

$$\text{I balanced modulator} = (-1)(\sin \omega_c t) = -1 \sin \omega_c t$$

$$\text{Q balanced modulator} = (-1)(\cos \omega_c t) = -1 \cos \omega_c t$$

and the output of the linear summer is

$$-1 \cos \omega_c t - 1 \sin \omega_c t = 1.414 \sin(\omega_c t - 135°)$$

For the remaining dibit codes (01, 10, and 11), the procedure is the same. The results are shown in Figure 18a.

In Figures 18b and c, it can be seen that with QPSK each of the four possible output phasors has exactly the same amplitude. Therefore, the binary information must be encoded entirely in the phase of the output signal. This constant amplitude characteristic is the most important characteristic of PSK that distinguishes it from QAM, which is explained later in this chapter. Also, from Figure 18b, it can be seen that the angular separation between any two adjacent phasors in QPSK is 90°. Therefore, a QPSK signal can undergo almost a +45° or −45° shift in phase during transmission and still retain the correct encoded information when demodulated at the receiver. Figure 19 shows the output phase-versus-time relationship for a QPSK modulator.

Binary input Q	Binary input I	QPSK output phase
0	0	−135°
0	1	−45°
1	0	+135°
1	1	+45°

(a)

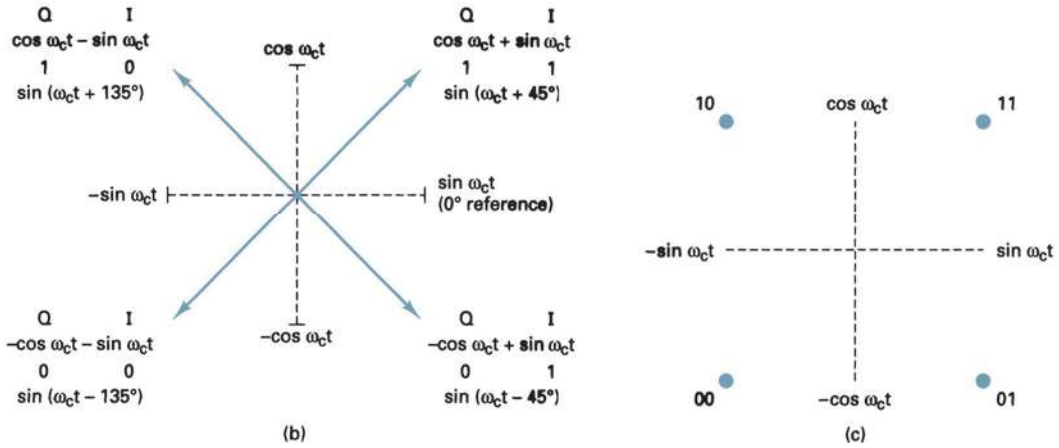


FIGURE 18 QPSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

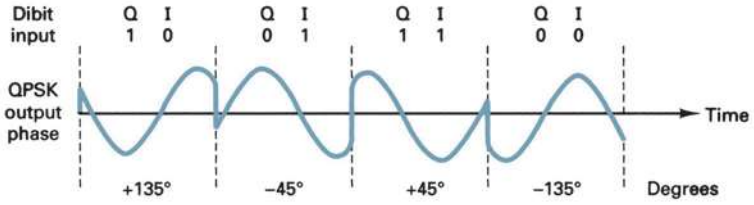


FIGURE 19 Output phase-versus-time relationship for a QPSK modulator

5-2-2 Bandwidth considerations of QPSK. With QPSK, because the input data are divided into two channels, the bit rate in either the I or the Q channel is equal to one-half of the input data rate ($f_b/2$). (Essentially, the bit splitter stretches the I and Q bits to twice their input bit length.) Consequently, the highest fundamental frequency present at the data input to the I or the Q balanced modulator is equal to one-fourth of the input data rate (one-half of $f_b/2 = f_b/4$). As a result, the output of the I and Q balanced modulators requires a minimum double-sided Nyquist bandwidth equal to one-half of the incoming bit rate (f_N = twice $f_b/4$ = $f_b/2$). Thus, with QPSK, a bandwidth compression is realized (the minimum bandwidth is less than the incoming bit rate). Also, because the QPSK output signal does not change phase until two bits (a dibit) have been clocked into the bit splitter, the fastest output rate of change (baud) is also equal to one-half of the input bit rate. As with BPSK, the minimum bandwidth and the baud are equal. This relationship is shown in Figure 20.

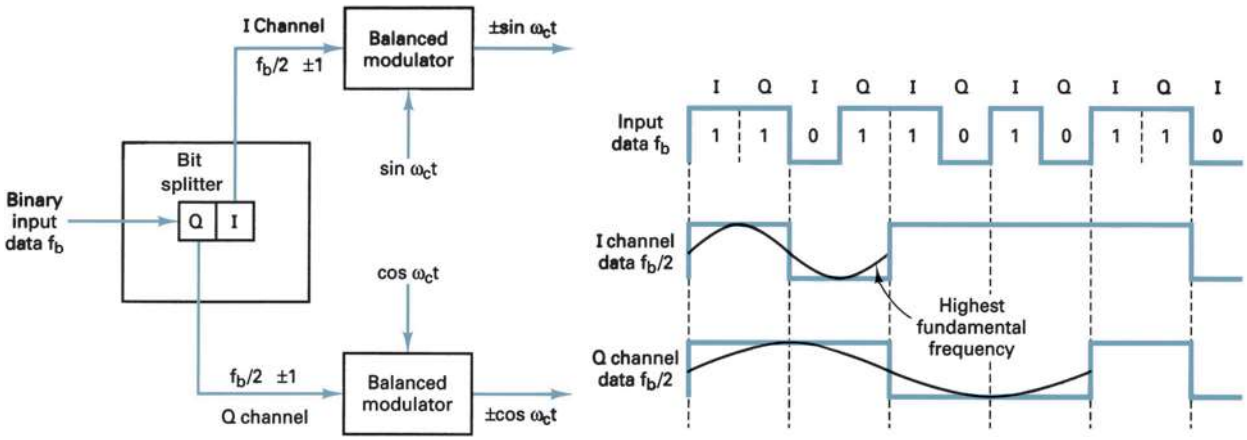


FIGURE 20 Bandwidth considerations of a QPSK modulator

In Figure 20, it can be seen that the worse-case input condition to the I or Q balanced modulator is an alternative 1/0 pattern, which occurs when the binary input data have a 1100 repetitive pattern. One cycle of the fastest binary transition (a 1/0 sequence) in the I or Q channel takes the same time as four input data bits. Consequently, the highest fundamental frequency at the input and fastest rate of change at the output of the balanced modulators is equal to one-fourth of the binary input bit rate.

The output of the balanced modulators can be expressed mathematically as

$$\text{output} = (\sin \omega_a t)(\sin \omega_c t) \tag{22}$$

where

$$\underbrace{\omega_a t = 2\pi \frac{f_b}{4} t}_{\text{modulating signal}} \quad \text{and} \quad \underbrace{\omega_c t = 2\pi f_c}_{\text{carrier}}$$

Thus,

$$\text{output} = \left(\sin 2\pi \frac{f_b}{4} t\right)(\sin 2\pi f_c t)$$

$$\frac{1}{2}\cos 2\pi\left(f_c - \frac{f_b}{4}\right)t - \frac{1}{2}\cos 2\pi\left(f_c + \frac{f_b}{4}\right)t$$

The output frequency spectrum extends from $f_c + f_b/4$ to $f_c - f_b/4$, and the minimum bandwidth (f_N) is

$$\left(f_c + \frac{f_b}{4}\right) - \left(f_c - \frac{f_b}{4}\right) = \frac{2f_b}{4} = \frac{f_b}{2}$$

Example 6

For a QPSK modulator with an input data rate (f_b) equal to 10 Mbps and a carrier frequency of 70 MHz, determine the minimum double-sided Nyquist bandwidth (f_N) and the baud. Also, compare the results with those achieved with the BPSK modulator in Example 4. Use the QPSK block diagram shown in Figure 17 as the modulator model.

Solution The bit rate in both the I and Q channels is equal to one-half of the transmission bit rate, or

$$f_{bQ} = f_{bI} = \frac{f_b}{2} = \frac{10 \text{ Mbps}}{2} = 5 \text{ Mbps}$$

The highest fundamental frequency presented to either balanced modulator is

$$f_a = \frac{f_{bQ}}{2} \text{ or } \frac{f_{bI}}{2} = \frac{5 \text{ Mbps}}{2} = 2.5 \text{ MHz}$$

The output wave from each balanced modulator is

$$(\sin 2\pi f_a t)(\sin 2\pi f_c t)$$

$$\frac{1}{2}\cos 2\pi(f_c - f_a)t - \frac{1}{2}\cos 2\pi(f_c + f_a)t$$

$$\frac{1}{2}\cos 2\pi[(70 - 2.5) \text{ MHz}]t - \frac{1}{2}\cos 2\pi[(70 + 2.5) \text{ MHz}]t$$

$$\frac{1}{2}\cos 2\pi(67.5 \text{ MHz})t - \frac{1}{2}\cos 2\pi(72.5 \text{ MHz})t$$

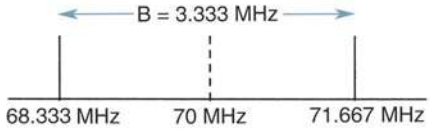
The minimum Nyquist bandwidth is

$$B = (72.5 - 67.5) \text{ MHz} = 5 \text{ MHz}$$

The symbol rate equals the bandwidth; thus,

$$\text{symbol rate} = 5 \text{ megabaud}$$

The output spectrum is as follows:



$$B = 5 \text{ MHz}$$

It can be seen that for the same input bit rate the minimum bandwidth required to pass the output of the QPSK modulator is equal to one-half of that required for the BPSK modulator in Example 4. Also, the baud rate for the QPSK modulator is one-half that of the BPSK modulator.

The minimum bandwidth for the QPSK system described in Example 6 can also be determined by simply substituting into Equation 10:

$$B = \frac{10 \text{ Mbps}}{2}$$
$$= 5 \text{ MHz}$$

5-2-3 QPSK receiver. The block diagram of a QPSK receiver is shown in Figure 21. The power splitter directs the input QPSK signal to the I and Q product detectors and the carrier recovery circuit. The carrier recovery circuit reproduces the original transmit carrier oscillator signal. The recovered carrier must be frequency and phase coherent with the transmit reference carrier. The QPSK signal is demodulated in the I and Q product detectors, which generate the original I and Q data bits. The outputs of the product detectors are fed to the bit combining circuit, where they are converted from parallel I and Q data channels to a single binary output data stream.

The incoming QPSK signal may be any one of the four possible output phases shown in Figure 18. To illustrate the demodulation process, let the incoming QPSK signal be $-\sin \omega_c t + \cos \omega_c t$. Mathematically, the demodulation process is as follows.

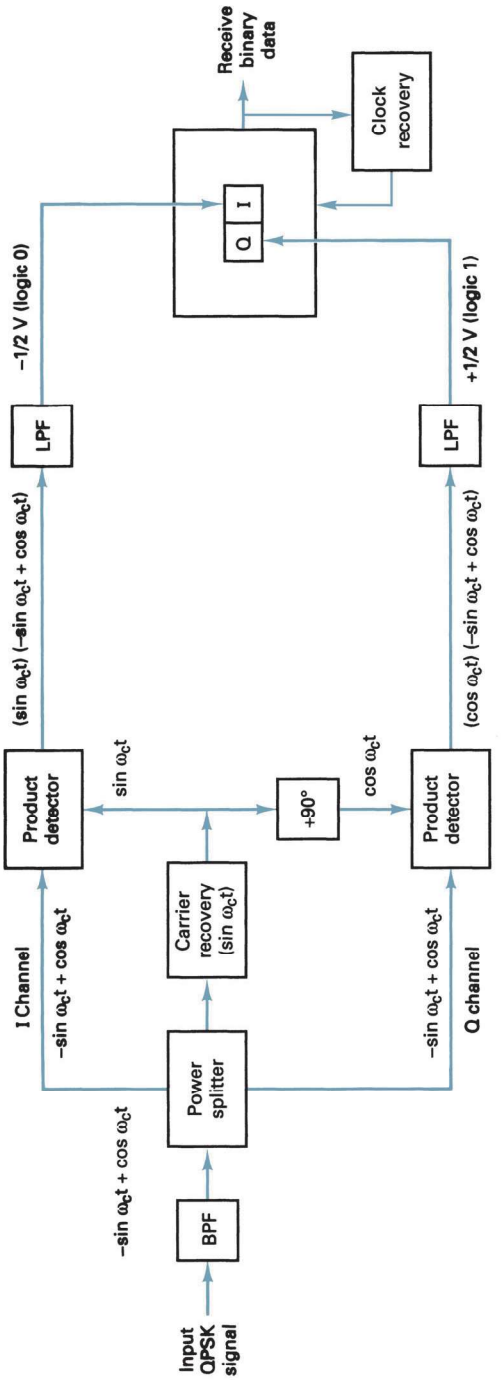


FIGURE 21 QPSK receiver

The receive QPSK signal ($-\sin \omega_c t + \cos \omega_c t$) is one of the inputs to the I product detector. The other input is the recovered carrier ($\sin \omega_c t$). The output of the I product detector is

$$\mathrm{I} = \underbrace{(-\sin \omega_c t + \cos \omega_c t)}_{\text{QPSK input signal}} \underbrace{(\sin \omega_c t)}_{\text{carrier}} \tag{23}$$

$$= (-\sin \omega_c t)(\sin \omega_c t) + (\cos \omega_c t)(\sin \omega_c t)$$

$$= -\sin^2 \omega_c t + (\cos \omega_c t)(\sin \omega_c t)$$

$$= -\frac{1}{2}(1 - \cos 2\omega_c t) + \frac{1}{2}\sin(\omega_c + \omega_c)t + \frac{1}{2}\sin(\omega_c - \omega_c)t$$

$$\mathrm{I} = -\frac{1}{2} + \frac{1}{2}\cos 2\omega_c t + \frac{1}{2}\sin 2\omega_c t + \frac{1}{2}\sin 0$$

(filtered out) (equals 0)

$$= -\frac{1}{2}\mathrm{V}\ (\text{logic } 0)$$

Again, the receive QPSK signal ($-\sin \omega_c t + \cos \omega_c t$) is one of the inputs to the Q product detector. The other input is the recovered carrier shifted 90° in phase ($\cos \omega_c t$). The output of the Q product detector is

$$\mathrm{Q} = \underbrace{(-\sin \omega_c t + \cos \omega_c t)}_{\text{QPSK input signal}} \underbrace{(\cos \omega_c t)}_{\text{carrier}} \tag{24}$$

$$= \cos^2 \omega_c t - (\sin \omega_c t)(\cos \omega_c t)$$

$$= \frac{1}{2}(1 + \cos 2\omega_c t) - \frac{1}{2}\sin(\omega_c + \omega_c)t - \frac{1}{2}\sin(\omega_c - \omega_c)t$$

$$\mathrm{Q} = \frac{1}{2} + \frac{1}{2}\cos 2\omega_c t - \frac{1}{2}\sin 2\omega_c t - \frac{1}{2}\sin 0$$

(filtered out) (equals 0)

$$= \frac{1}{2}\mathrm{V}(\text{logic } 1)$$

The demodulated I and Q bits (0 and 1, respectively) correspond to the constellation diagram and truth table for the QPSK modulator shown in Figure 18.

5-2-4 Offset QPSK. *Offset QPSK* (OQPSK) is a modified form of QPSK where the bit waveforms on the I and Q channels are offset or shifted in phase from each other by one-half of a bit time.

Figure 22 shows a simplified block diagram, the bit sequence alignment, and the constellation diagram for a OQPSK modulator. Because changes in the I channel occur at the midpoints of the Q channel bits and vice versa, there is never more than a single bit change in the dibit code and, therefore, there is never more than a 90° shift in the output phase. In conventional QPSK, a change in the input dibit from 00 to 11 or 01 to 10 causes a corresponding 180° shift in the output phase. Therefore, an advantage of OQPSK is the limited phase shift that must be imparted during modulation. A disadvantage of OQPSK is

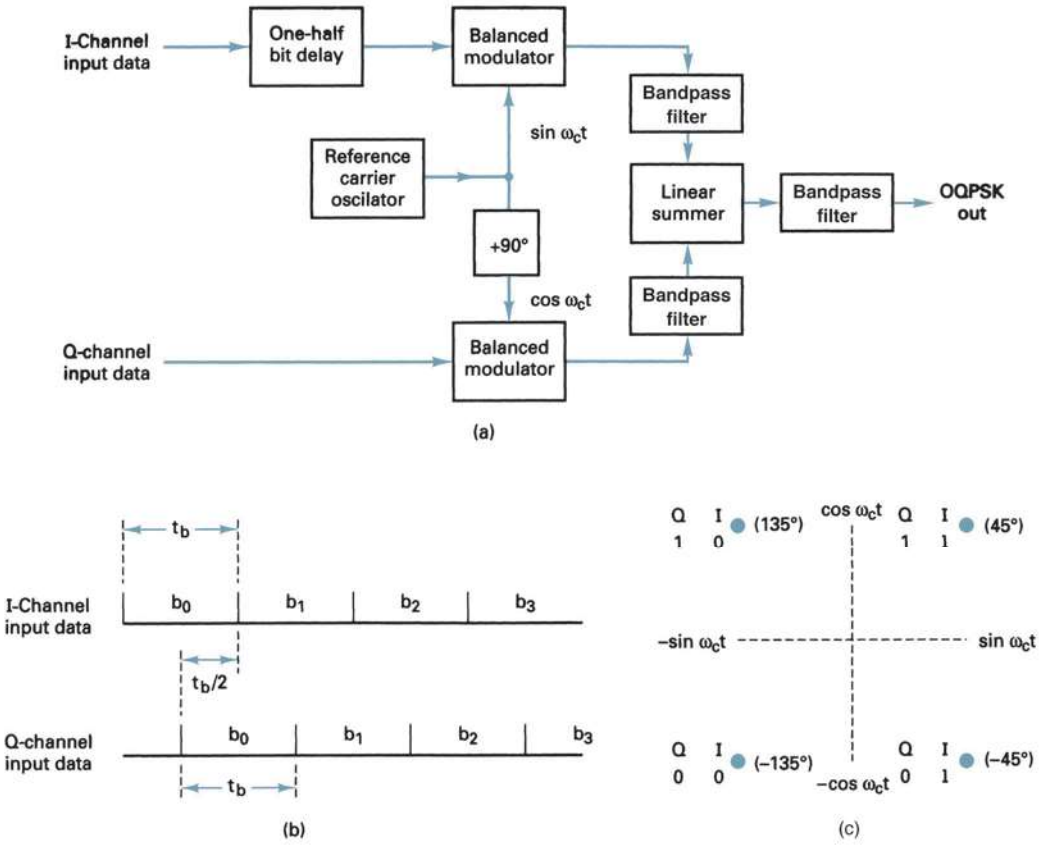


FIGURE 22 Offset keyed (OQPSK): (a) block diagram; (b) bit alignment; (c) constellation diagram

that changes in the output phase occur at twice the data rate in either the I or Q channels. Consequently, with OQPSK the baud and minimum bandwidth are twice that of conventional QPSK for a given transmission bit rate. OQPSK is sometimes called OKQPSK (*offset-keyed QPSK*).

5-3 8-PSK

With *8-PSK,* three bits are encoded, forming tribits and producing eight different output phases. With 8-PSK, $n = 3$, $M = 8$, and there are eight possible output phases. To encode eight different phases, the incoming bits are encoded in groups of three, called tribits ($2^3 = 8$).

5-3-1 8-PSK transmitter. A block diagram of an 8-PSK modulator is shown in Figure 23. The incoming serial bit stream enters the bit splitter, where it is converted to a parallel, three-channel output (the I or in-phase channel, the Q or in-quadrature channel, and the C or control channel). Consequently, the bit rate in each of the three channels is $f_b/3$. The bits in the I and C channels enter the I channel 2-to-4-level converter, and the bits in the Q and $\overline{C}$ channels enter the Q channel 2-to-4-level converter. Essentially, the 2-to-4-level converters are parallel-input *digital-to-analog converters* (DACs). With two input bits, four output voltages are possible. The algorithm for the DACs is quite simple. The I or Q bit determines the polarity of the output analog signal (logic 1 = +V and logic 0 = −V), whereas the C or $\overline{C}$ bit determines the magni-

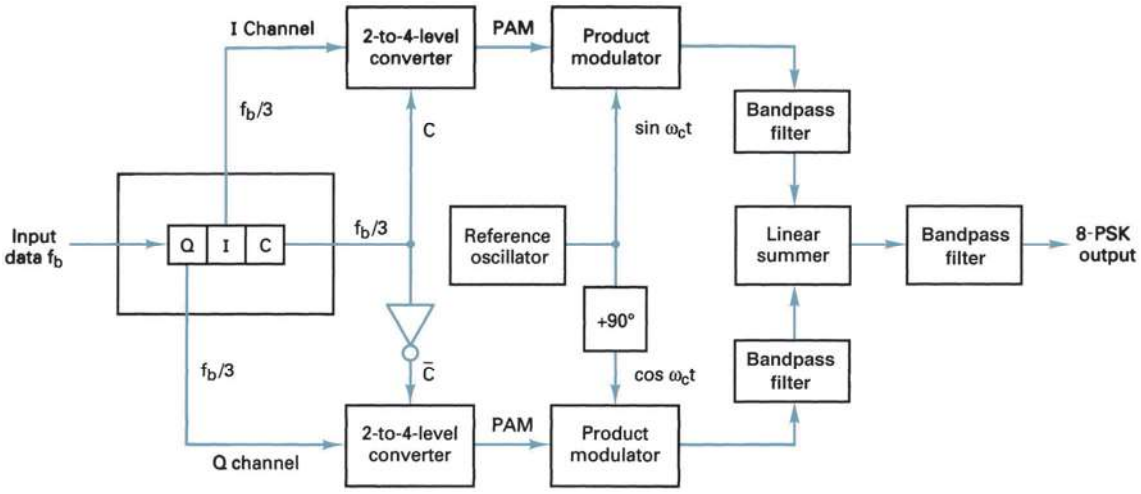


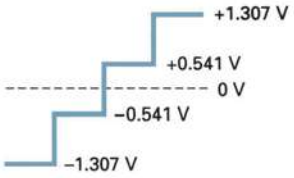
FIGURE 23 8-PSK modulator

I	C	Output
0	0	−0.541 V
0	1	−1.307 V
1	0	+0.541 V
1	1	+1.307 V

(a)

Q	$\bar{C}$	Output
0	1	−1.307 V
0	0	−0.541 V
1	1	+1.307 V
1	0	+0.541 V

(b)



(c)

FIGURE 24 I- and Q-channel 2-to-4-level converters: (a) I-channel truth table; (b) Q-channel truth table; (c) PAM levels

tude (logic 1 = 1.307 V and logic 0 = 0.541 V). Consequently, with two magnitudes and two polarities, four different output conditions are possible.

Figure 24 shows the truth table and corresponding output conditions for the 2-to-4-level converters. Because the C and $\bar{C}$ bits can never be the same logic state, the outputs from the I and Q 2-to-4-level converters can never have the same magnitude, although they can have the same polarity. The output of a 2-to-4-level converter is an *M*-ary, *pulse-amplitude-modulated* (PAM) signal where $M = 4$.

Example 7

For a tribit input of Q = 0, 1 = 0, and C = 0 (000), determine the output phase for the 8-PSK modulator shown in Figure 23.

Solution The inputs to the I channel 2-to-4-level converter are I = 0 and C = 0. From Figure 24 the output is −0.541 V. The inputs to the Q channel 2-to-4-level converter are Q = 0 and $\bar{C} = 1$. Again from Figure 24, the output is −1.307 V.

Thus, the two inputs to the I channel product modulators are −0.541 and sin $\omega_c t$. The output is

$$I = (-0.541)(\sin \omega_c t) = -0.541 \sin \omega_c t$$

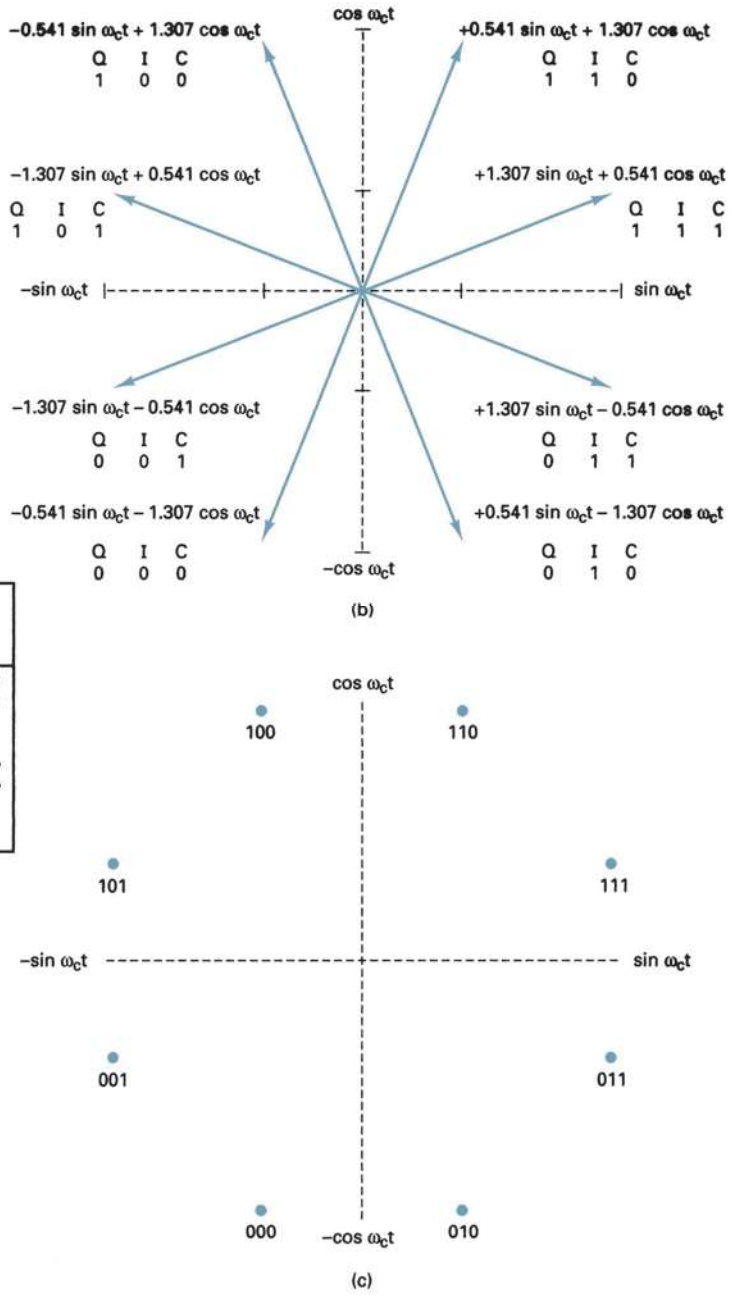
The two inputs to the Q channel product modulator are −1.307 V and cos $\omega_c t$. The output is

$$Q = (-1.307)(\cos \omega_c t) = -1.307 \cos \omega_c t$$

The outputs of the I and Q channel product modulators are combined in the linear summer and produce a modulated output of

$$\text{summer output} = -0.541 \sin \omega_c t - 1.307 \cos \omega_c t$$
$$= 1.41 \sin(\omega_c t - 112.5°)$$

For the remaining tribit codes (001, 010, 011, 100, 101, 110, and 111), the procedure is the same. The results are shown in Figure 25.



Binary input Q I C	8-PSK output phase
0 0 0	−112.5°
0 0 1	−157.5°
0 1 0	−67.5°
0 1 1	−22.5°
1 0 0	+112.5°
1 0 1	+157.5°
1 1 0	+67.5°
1 1 1	+22.5°

(a)

FIGURE 25 8-PSK modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

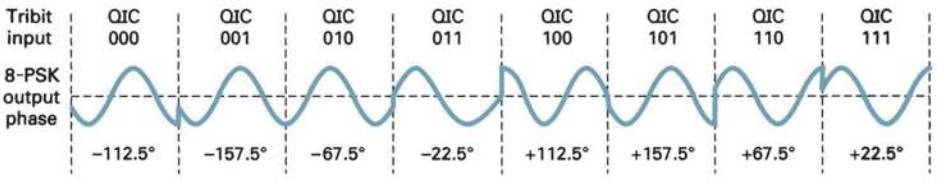


FIGURE 26 Output phase-versus-time relationship for an 8-PSK modulator

From Figure 25, it can be seen that the angular separation between any two adjacent phasors is 45°, half what it is with QPSK. Therefore, an 8-PSK signal can undergo almost a ±22.5° phase shift during transmission and still retain its integrity. Also, each phasor is of equal magnitude; the tribit condition (actual information) is again contained only in the phase of the signal. The PAM levels of 1.307 and 0.541 are relative values. Any levels may be used as long as their ratio is 0.541/1.307 and their arc tangent is equal to 22.5°. For example, if their values were doubled to 2.614 and 1.082, the resulting phase angles would not change, although the magnitude of the phasor would increase proportionally.

It should also be noted that the tribit code between any two adjacent phases changes by only one bit. This type of code is called the *Gray code* or, sometimes, the *maximum distance code.* This code is used to reduce the number of transmission errors. If a signal were to undergo a phase shift during transmission, it would most likely be shifted to an adjacent phasor. Using the Gray code results in only a single bit being received in error.

Figure 26 shows the output phase-versus-time relationship of an 8-PSK modulator.

5-3-2 Bandwidth considerations of 8-PSK. With 8-PSK, because the data are divided into three channels, the bit rate in the I, Q, or C channel is equal to one-third of the binary input data rate ($f_b/3$). (The bit splitter stretches the I, Q, and C bits to three times their input bit length.) Because the I, Q, and C bits are outputted simultaneously and in parallel, the 2-to-4-level converters also see a change in their inputs (and consequently their outputs) at a rate equal to $f_b/3$.

Figure 27 shows the bit timing relationship between the binary input data; the I, Q, and C channel data; and the I and Q PAM signals. It can be seen that the highest fundamental frequency in the I, Q, or C channel is equal to one-sixth the bit rate of the binary input (one cycle in the I, Q, or C channel takes the same amount of time as six input bits). Also, the highest fundamental frequency in either PAM signal is equal to one-sixth of the binary input bit rate.

With an 8-PSK modulator, there is one change in phase at the output for every three data input bits. Consequently, the baud for 8 PSK equals $f_b/3$, the same as the minimum bandwidth. Again, the balanced modulators are product modulators; their outputs are the product of the carrier and the PAM signal. Mathematically, the output of the balanced modulators is

$$\theta = (X \sin \omega_a t)(\sin \omega_c t) \tag{25}$$

where $\underbrace{\omega_a t = 2\pi \frac{f_b}{6} t}_{\text{modulating signal}}$ and $\underbrace{\omega_c t = 2\pi f_c t}_{\text{carrier}}$

and $X = \pm 1.307$ or ± 0.541

Thus,
$$\theta = \left(X \sin 2\pi \frac{f_b}{6} t\right)(\sin 2\pi f_c t)$$
$$= \frac{X}{2} \cos 2\pi \left(f_c - \frac{f_b}{6}\right) t - \frac{X}{2} \cos 2\pi \left(f_c + \frac{f_b}{6}\right) t$$

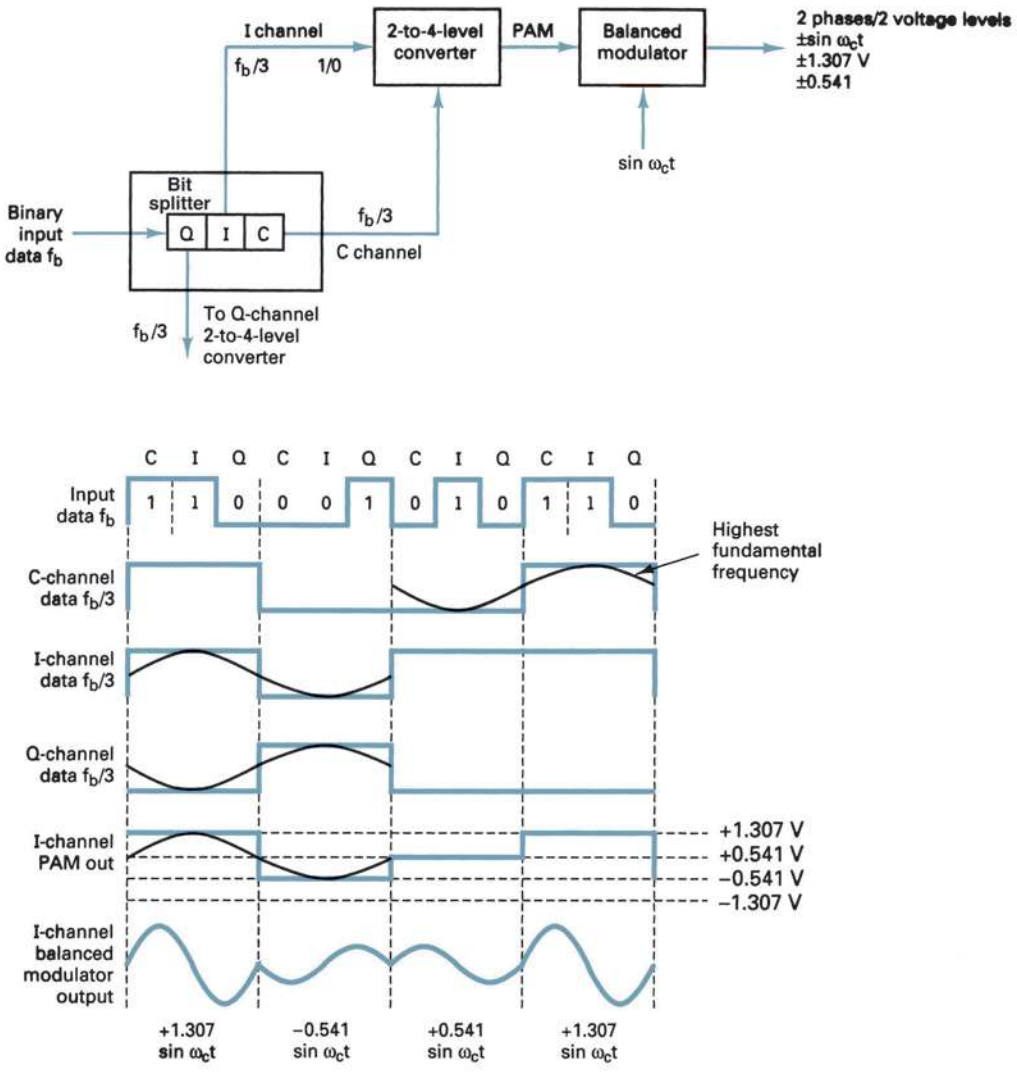


FIGURE 27 Bandwidth considerations of an 8-PSK modulator

The output frequency spectrum extends from $f_c + f_b/6$ to $f_c - f_b/6$, and the minimum bandwidth (f_N) is

$$\left(f_c + \frac{f_b}{6}\right) - \left(f_c - \frac{f_b}{6}\right) = \frac{2f_b}{6} = \frac{f_b}{3}$$

Example 8

For an 8-PSK modulator with an input data rate (f_b) equal to 10 Mbps and a carrier frequency of 70 MHz, determine the minimum double-sided Nyquist bandwidth (f_N) and the baud. Also, compare the results with those achieved with the BPSK and QPSK modulators in Examples 4 and 6. Use the 8-PSK block diagram shown in Figure 23 as the modulator model.

Solution The bit rate in the I, Q, and C channels is equal to one-third of the input bit rate, or

$$f_{bC} = f_{bQ} = f_{bI} = \frac{10 \text{ Mbps}}{3} = 3.33 \text{ Mbps}$$

Therefore, the fastest rate of change and highest fundamental frequency presented to either balanced modulator is

$$f_a = \frac{f_{bC}}{2} \text{ or } \frac{f_{bQ}}{2} \text{ or } \frac{f_{bI}}{2} = \frac{3.33 \text{ Mbps}}{2} = 1.667 \text{ Mbps}$$

The output wave from the balance modulators is

$$(\sin 2\pi f_a t)(\sin 2\pi f_c t)$$

$$\frac{1}{2}\cos 2\pi(f_c - f_a)t - \frac{1}{2}\cos 2\pi(f_c + f_a)t$$

$$\frac{1}{2}\cos 2\pi[(70 - 1.667)\text{ MHz}]t - \frac{1}{2}\cos 2\pi[(70 + 1.667)\text{ MHz}]t$$

$$\frac{1}{2}\cos 2\pi(68.333\text{ MHz})t - \frac{1}{2}\cos 2\pi(71.667\text{ MHz})t$$

The minimum Nyquist bandwidth is

$$B = (71.667 - 68.333)\text{ MHz} = 3.333\text{ MHz}$$

The minimum bandwidth for the 8-PSK can also be determined by simply substituting into Equation 10:

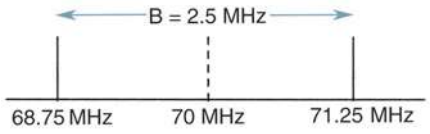
$$B = \frac{10 \text{ Mbps}}{3}$$

$$= 3.33 \text{ MHz}$$

Again, the baud equals the bandwidth; thus,

$$\text{baud} = 3.333 \text{ megabaud}$$

The output spectrum is as follows:



$$B = 3.333 \text{ MHz}$$

It can be seen that for the same input bit rate the minimum bandwidth required to pass the output of an 8-PSK modulator is equal to one-third that of the BPSK modulator in Example 4 and 50% less than that required for the QPSK modulator in Example 6. Also, in each case the baud has been reduced by the same proportions.

5-3-3 8-PSK receiver. Figure 28 shows a block diagram of an 8-PSK receiver. The power splitter directs the input 8-PSK signal to the I and Q product detectors and the carrier recovery circuit. The carrier recovery circuit reproduces the original reference oscillator signal. The incoming 8-PSK signal is mixed with the recovered carrier in the I product detector and with a quadrature carrier in the Q product detector. The outputs of the product detectors are 4-level PAM signals that are fed to the 4-to-2-level *analog-to-digital converters* (ADCs). The outputs from the I channel 4-to-2-level converter are the I and C bits, whereas the outputs from the Q channel 4-to-2-level converter are the Q and $\overline{C}$ bits. The parallel-to-serial logic circuit converts the I/C and Q/$\overline{C}$ bit pairs to serial I, Q, and C output data streams.

5-4 16-PSK

16-PSK is an *M*-ary encoding technique where $M = 16$; there are 16 different output phases possible. With 16-PSK, four bits (called *quadbits*) are combined, producing 16 different output phases. With 16-PSK, $n = 4$ and $M = 16$; therefore, the minimum bandwidth and

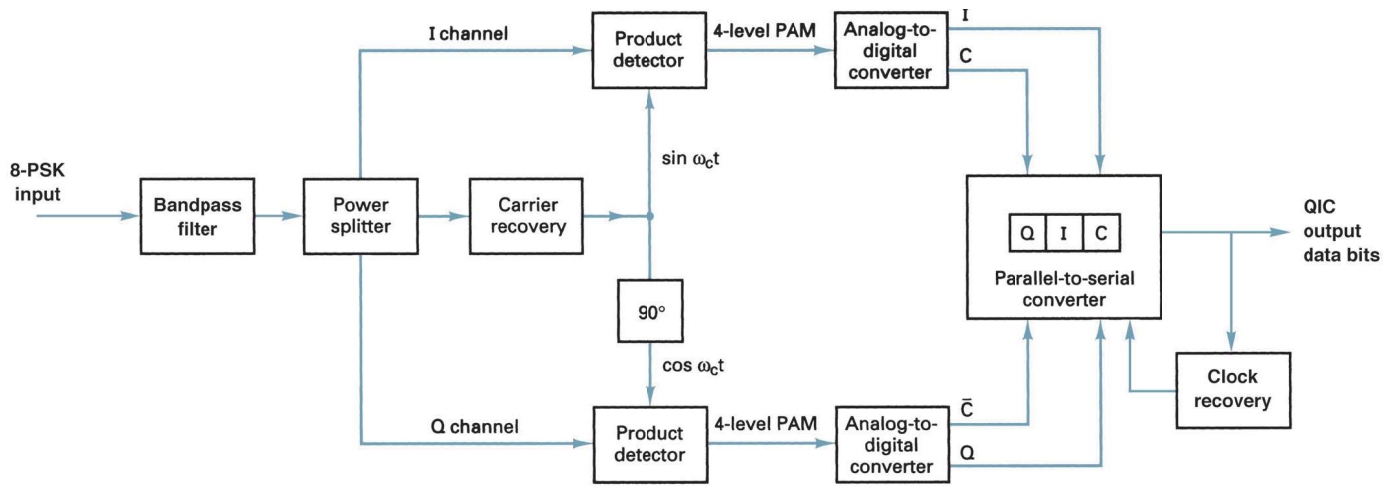
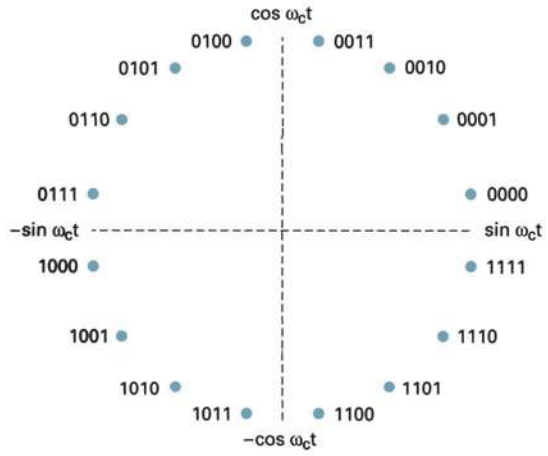


FIGURE 28 8-PSK receiver

Bit code	Phase	Bit code	Phase
0000	11.25°	1000	191.25°
0001	33.75°	1001	213.75°
0010	56.25°	1010	236.25°
0011	78.75°	1011	258.75°
0100	101.25°	1100	281.25°
0101	123.75°	1101	303.75°
0110	146.25°	1110	326.25°
0111	168.75°	1111	348.75°

(a)



(b)

FIGURE 29 16-PSK: (a) truth table; (b) constellation diagram

baud equal one-fourth the bit rate ($f_b/4$). Figure 29 shows the truth table and constellation diagram for 16-PSK, respectively. Comparing Figures 18, 25, and 29 shows that as the level of encoding increases (i.e., the values of n and M increase), more output phases are possible and the closer each point on the constellation diagram is to an adjacent point. With 16-PSK, the angular separation between adjacent output phases is only 22.5°. Therefore, 16-PSK can undergo only a 11.25° phase shift during transmission and still retain its integrity. For an M-ary PSK system with 64 output phases ($n = 6$), the angular separation between adjacent phases is only 5.6°. This is an obvious limitation in the level of encoding (and bit rates) possible with PSK, as a point is eventually reached where receivers cannot discern the phase of the received signaling element. In addition, phase impairments inherent on communications lines have a tendency to shift the phase of the PSK signal, destroying its integrity and producing errors.

6 QUADRATURE-AMPLITUDE MODULATION

Quadrature-amplitude modulation (QAM) is a form of digital modulation similar to PSK except the digital information is contained in both the amplitude and the phase of the transmitted carrier. With QAM, amplitude and phase-shift keying are combined in such a way that the positions of the signaling elements on the constellation diagrams are optimized to achieve the greatest distance between elements, thus reducing the likelihood of one element being misinterpreted as another element. Obviously, this reduces the likelihood of errors occurring.

6-1 8-QAM

8-QAM is an M-ary encoding technique where $M = 8$. Unlike 8-PSK, the output signal from an 8-QAM modulator is not a constant-amplitude signal.

6-1-1 8-QAM transmitter. Figure 30a shows the block diagram of an 8-QAM transmitter. As you can see, the only difference between the 8-QAM transmitter and the 8-PSK transmitter shown in Figure 23 is the omission of the inverter between the C channel and the Q product modulator. As with 8-PSK, the incoming data are divided into groups of three bits (tribits): the I, Q, and C bit streams, each with a bit rate equal to one-third of

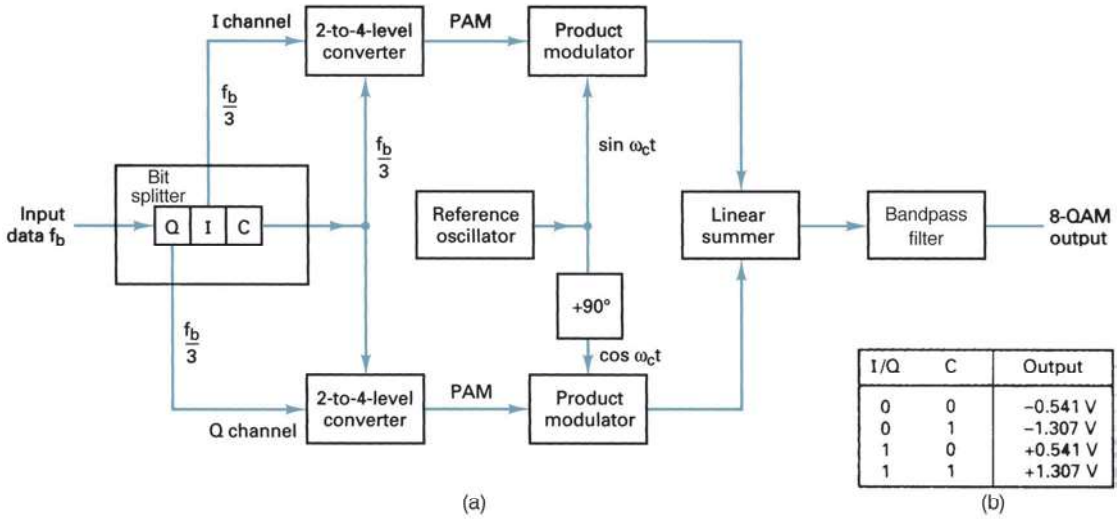


FIGURE 30 8-QAM transmitter: (a) block diagram; (b) truth table 4 level converters

the incoming data rate. Again, the I and Q bits determine the polarity of the PAM signal at the output of the 2-to-4-level converters, and the C channel determines the magnitude. Because the C bit is fed uninverted to both the I and the Q channel 2-to-4-level converters, the magnitudes of the I and Q PAM signals are always equal. Their polarities depend on the logic condition of the I and Q bits and, therefore, may be different. Figure 30b shows the truth table for the I and Q channel 2-to-4-level converters; they are identical.

Example 9

For a tribit input of Q = 0, I = 0, and C = 0 (000), determine the output amplitude and phase for the 8-QAM transmitter shown in Figure 30a.

Solution The inputs to the I channel 2-to-4-level converter are I = 0 and C = 0. From Figure 30b, the output is −0.541 V. The inputs to the Q channel 2-to-4-level converter are Q = 0 and C = 0. Again from Figure 30b, the output is −0.541 V.

Thus, the two inputs to the I channel product modulator are −0.541 and sin $\omega_c t$. The output is

$$I = (-0.541)(\sin \omega_c t) = -0.541 \sin \omega_c t$$

The two inputs to the Q channel product modulator are −0.541 and cos $\omega_c t$. The output is

$$Q = (-0.541)(\cos \omega_c t) = -0.541 \cos \omega_c t$$

The outputs from the I and Q channel product modulators are combined in the linear summer and produce a modulated output of

$$\text{summer output} = -0.541 \sin \omega_c t - 0.541 \cos \omega_c t$$
$$= 0.765 \sin(\omega_c t - 135°)$$

For the remaining tribit codes (001, 010, 011, 100, 101, 110, and 111), the procedure is the same. The results are shown in Figure 31.

Figure 32 shows the output phase-versus-time relationship for an 8-QAM modulator. Note that there are two output amplitudes, and only four phases are possible.

6-1-2 Bandwidth considerations of 8-QAM. In 8-QAM, the bit rate in the I and Q channels is one-third of the input binary rate, the same as in 8-PSK. As a result, the highest fundamental modulating frequency and fastest output rate of change in 8-QAM are the same as with 8-PSK. Therefore, the minimum bandwidth required for 8-QAM is $f_b/3$, the same as in 8-PSK.

Binary input			8-QAM output	
Q	I	C	Amplitude	Phase
0	0	0	0.765 V	−135°
0	0	1	1.848 V	−135°
0	1	0	0.765 V	−45°
0	1	1	1.848 V	−45°
1	0	0	0.765 V	+135°
1	0	1	1.848 V	+135°
1	1	0	0.765 V	+45°
1	1	1	1.848 V	+45°

(a)

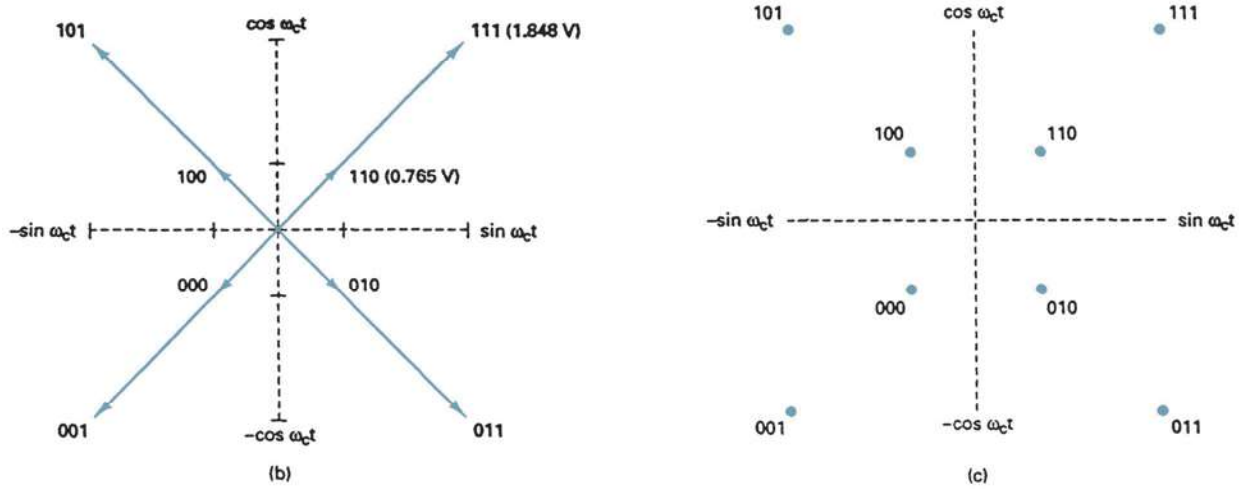


FIGURE 31 8-QAM modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

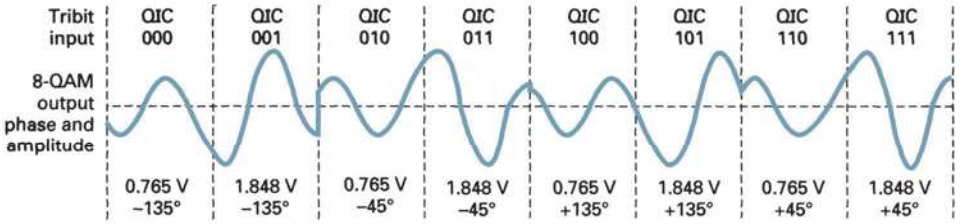


FIGURE 32 Output phase and amplitude-versus-time relationship for 8-QAM

6-1-3 8-QAM receiver. An 8-QAM receiver is almost identical to the 8-PSK receiver shown in Figure 28. The differences are the PAM levels at the output of the product detectors and the binary signals at the output of the analog-to-digital converters. Because there are two transmit amplitudes possible with 8-QAM that are different from those achievable with 8-PSK, the four demodulated PAM levels in 8-QAM are different from those in 8-PSK. Therefore, the conversion factor for the analog-to-digital converters must also be different. Also, with 8-QAM the binary output signals from the I channel analog-to-digital converter are the I and C bits, and the binary output signals from the Q channel analog-to-digital converter are the Q and C bits.

6-2 16-QAM

As with the 16-PSK, *16-QAM* is an *M*-ary system where $M = 16$. The input data are acted on in groups of four ($2^4 = 16$). As with 8-QAM, both the phase and the amplitude of the transmit carrier are varied.

6-2-1 QAM transmitter. The block diagram for a 16-QAM transmitter is shown in Figure 33. The input binary data are divided into four channels: I, I′, Q, and Q′. The bit rate in each channel is equal to one-fourth of the input bit rate ($f_b/4$). Four bits are serially clocked into the bit splitter; then they are outputted simultaneously and in parallel with the I, I′, Q, and Q′ channels. The I and Q bits determine the polarity at the output of the 2-to-4-level converters (a logic 1 = positive and a logic 0 = negative). The I′ and Q′ bits determine the magnitude (a logic I = 0.821 V and a logic 0 = 0.22 V). Consequently, the 2-to-4-level converters generate a 4-level PAM signal. Two polarities and two magnitudes are possible at the output of each 2-to-4-level converter. They are 0.22 V and ±0.821 V.

The PAM signals modulate the in-phase and quadrature carriers in the product modulators. Four outputs are possible for each product modulator. For the I product modulator, they are $+0.821 \sin \omega_c t$, $-0.821 \sin \omega_c t$, $+0.22 \sin \omega_c t$, and $-0.22 \sin \omega_c t$. For the Q product modulator, they are $+0.821 \cos \omega_c t$, $+0.22 \cos \omega_c t$, $-0.821 \cos \omega_c t$, and $-0.22 \cos \omega_c t$. The linear summer combines the outputs from the I and Q channel product modulators and produces the 16 output conditions necessary for 16-QAM. Figure 34 shows the truth table for the I and Q channel 2-to-4-level converters.

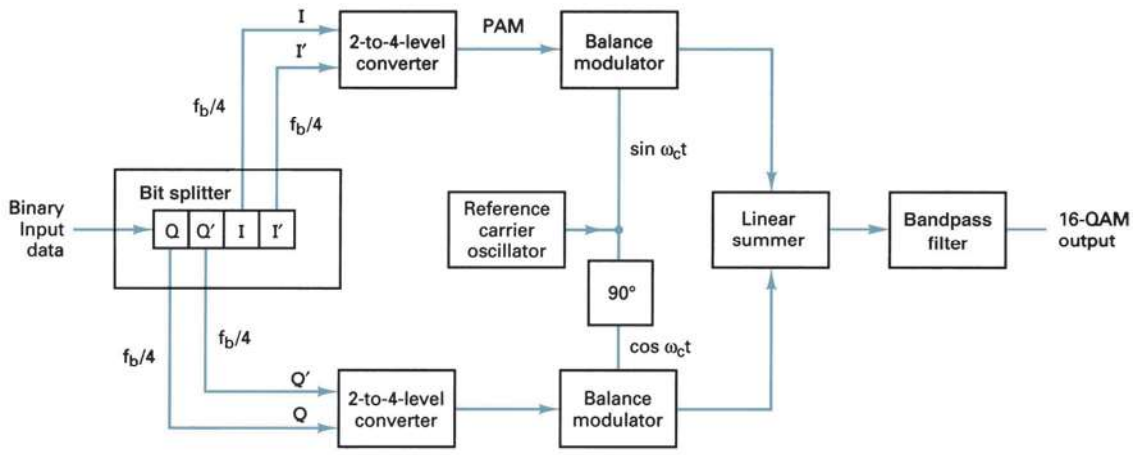


FIGURE 33 16-QAM transmitter block diagram

I	I′	Output
0	0	−0.22 V
0	1	−0.821 V
1	0	+0.22 V
1	1	+0.821 V

(a)

Q	Q′	Output
0	0	−0.22 V
0	1	−0.821 V
1	0	+0.22 V
1	1	+0.821 V

(b)

FIGURE 34 Truth tables for the I- and Q-channel 2-to-4-level converters: (a) I channel; (b) Q channel

Example 10

For a quadbit input of I = 0, I′ = 0, Q = 0, and Q′ = 0 (0000), determine the output amplitude and phase for the 16-QAM modulator shown in Figure 33.

Solution The inputs to the I channel 2-to-4-level converter are I = 0 and I′ = 0. From Figure 34, the output is −0.22 V. The inputs to the Q channel 2-to-4-level converter are Q = 0 and Q′ = 0. Again from Figure 34, the output is −0.22 V.

Thus, the two inputs to the I channel product modulator are −0.22 V and sin $\omega_c t$. The output is

$$I = (-0.22)(\sin \omega_c t) = -0.22 \sin \omega_c t$$

The two inputs to the Q channel product modulator are −0.22 V and cos $\omega_c t$. The output is

$$Q = (-0.22)(\cos \omega_c t) = -0.22 \cos \omega_c t$$

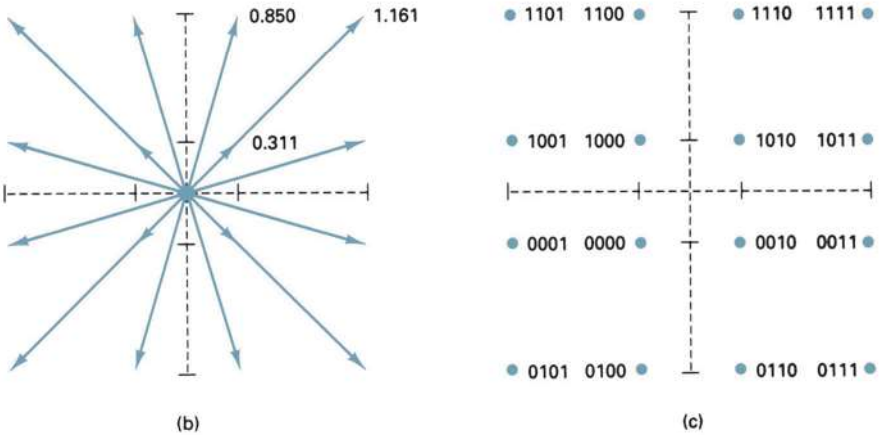
The outputs from the I and Q channel product modulators are combined in the linear summer and produce a modulated output of

$$\text{summer output} = -0.22 \sin \omega_c t - 0.22 \cos \omega_c t$$
$$= 0.311 \sin(\omega_c t - 135°)$$

For the remaining quadbit codes, the procedure is the same. The results are shown in Figure 35.

Binary input				16-QAM output	
Q	Q′	I	I′		
0	0	0	0	0.311 V	−135°
0	0	0	1	0.850 V	−165°
0	0	1	0	0.311 V	−45°
0	0	1	1	0.850 V	−15°
0	1	0	0	0.850 V	−105°
0	1	0	1	1.161 V	−135°
0	1	1	0	0.850 V	−75°
0	1	1	1	1.161 V	−45°
1	0	0	0	0.311 V	135°
1	0	0	1	0.850 V	165°
1	0	1	0	0.311 V	45°
1	0	1	1	0.850 V	15°
1	1	0	0	0.850 V	105°
1	1	0	1	1.161 V	135°
1	1	1	0	0.850 V	75°
1	1	1	1	1.161 V	45°

(a)



(b) (c)

FIGURE 35 16-QAM modulator: (a) truth table; (b) phasor diagram; (c) constellation diagram

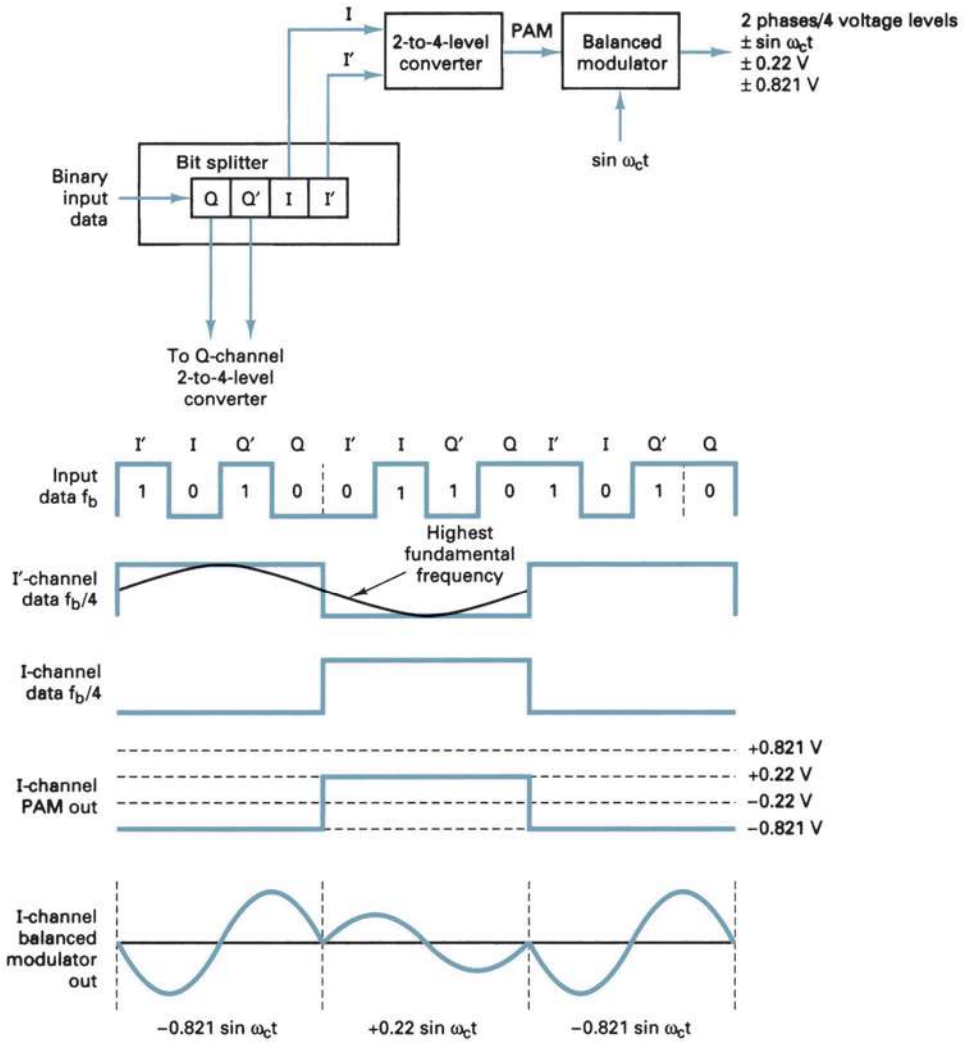


FIGURE 36 Bandwidth considerations of a 16-QAM modulator

6-2-2 Bandwidth considerations of 16-QAM. With a 16-QAM, because the input data are divided into four channels, the bit rate in the I, I′, Q, or Q′ channel is equal to one-fourth of the binary input data rate ($f_b/4$). (The bit splitter stretches the I, I′, Q, and Q′ bits to four times their input bit length.) Also, because the I, I′, Q, and Q′ bits are outputted simultaneously and in parallel, the 2-to-4-level converters see a change in their inputs and outputs at a rate equal to one-fourth of the input data rate.

Figure 36 shows the bit timing relationship between the binary input data; the I, I′, Q, and Q′ channel data; and the I PAM signal. It can be seen that the highest fundamental frequency in the I, I′, Q, or Q′ channel is equal to one-eighth of the bit rate of the binary input data (one cycle in the I, I′, Q, or Q′ channel takes the same amount of time as eight input bits). Also, the highest fundamental frequency of either PAM signal is equal to one-eighth of the binary input bit rate.

With a 16-QAM modulator, there is one change in the output signal (either its phase, amplitude, or both) for every four input data bits. Consequently, the baud equals $f_b/4$, the same as the minimum bandwidth.

Again, the balanced modulators are product modulators and their outputs can be represented mathematically as

$$\text{output} = (X \sin \omega_a t)(\sin \omega_c t) \tag{26}$$

where $$\underbrace{\omega_a t = 2\pi \frac{f_b}{8} t}_{\text{modulating signal}} \quad \text{and} \quad \underbrace{\omega_c t = 2\pi f_c t}_{\text{carrier}}$$

and $$X = \pm 0.22 \text{ or } \pm 0.821$$

Thus, $$\text{output} = \left(X \sin 2\pi \frac{f_b}{8} t\right)(\sin 2\pi f_c t)$$

$$= \frac{X}{2} \cos 2\pi \left(f_c - \frac{f_b}{8}\right) t = \frac{X}{2} \cos 2\pi \left(f_c + \frac{f_b}{8}\right) t$$

The output frequency spectrum extends from $f_c + f_b/8$ to $f_c - f_b/8$, and the minimum bandwidth (f_N) is

$$\left(f_c + \frac{f_b}{8}\right) - \left(f_c - \frac{f_b}{8}\right) = \frac{2f_b}{8} = \frac{f_b}{4}$$

Example 11

For a 16-QAM modulator with an input data rate (f_b) equal to 10 Mbps and a carrier frequency of 70 MHz, determine the minimum double-sided Nyquist frequency (f_N) and the baud. Also, compare the results with those achieved with the BPSK, QPSK, and 8-PSK modulators in Examples 4, 6, and 8. Use the 16-QAM block diagram shown in Figure 33 as the modulator model.

Solution The bit rate in the I, I′, Q, and Q′ channels is equal to one-fourth of the input bit rate, or

$$f_{bI} = f_{bI'} = f_{bQ} = f_{bQ'} = \frac{f_b}{4} = \frac{10 \text{ Mbps}}{4} = 2.5 \text{ Mbps}$$

Therefore, the fastest rate of change and highest fundamental frequency presented to either balanced modulator is

$$f_a = \frac{f_{bI}}{2} \text{ or } \frac{f_{bI'}}{2} \text{ or } \frac{f_{bQ}}{2} \text{ or } \frac{f_{bQ'}}{2} = \frac{2.5 \text{ Mbps}}{2} = 1.25 \text{ MHz}$$

The output wave from the balanced modulator is

$$(\sin 2\pi f_a t)(\sin 2\pi f_c t)$$

$$\frac{1}{2}\cos 2\pi (f_c - f_a) t - \frac{1}{2}\cos 2\pi (f_c + f_a) t$$

$$\frac{1}{2}\cos 2\pi [(70 - 1.25) \text{ MHz}] t - \frac{1}{2}\cos 2\pi [(70 + 1.25) \text{ MHz}] t$$

$$\frac{1}{2}\cos 2\pi (68.75 \text{ MHz}) t - \frac{1}{2}\cos 2\pi (71.25 \text{ MHz}) t$$

The minimum Nyquist bandwidth is

$$B = (71.25 - 68.75) \text{ MHz} = 2.5 \text{ MHz}$$

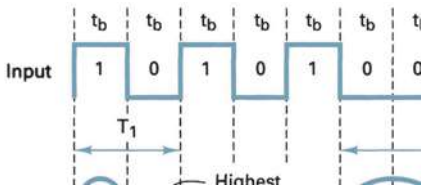
The minimum bandwidth for the 16-QAM can also be determined by simply substituting into Equation 10:

$$B = \frac{10 \text{ Mbps}}{4}$$
$$= 2.5 \text{ MHz}$$

The symbol rate equals the bandwidth; thus,

symbol rate = 2.5 megabaud

The output spectrum is as follows:



$B = 2.5$ MHz

For the same input bit rate, the minimum bandwidth required to pass the output of a 16-QAM modulator is equal to one-fourth that of the BPSK modulator, one-half that of QPSK, and 25% less than with 8-PSK. For each modulation technique, the baud is also reduced by the same proportions.

Example 12

For the following modulation schemes, construct a table showing the number of bits encoded, number of output conditions, minimum bandwidth, and baud for an information data rate of 12 kbps: QPSK, 8-PSK, 8-QAM, 16-PSK, and 16-QAM.

Solution

Modulation	n	M	B (Hz)	baud
QPSK	2	4	6000	6000
8-PSK	3	8	4000	4000
8-QAM	3	8	4000	4000
16-PSK	4	16	3000	3000
16-QAM	4	16	3000	3000

From Example 12, it can be seen that a 12-kbps data stream can be propagated through a narrower bandwidth using either 16-PSK or 16-QAM than with the lower levels of encoding.

Table 1 summarizes the relationship between the number of bits encoded, the number of output conditions possible, the minimum bandwidth, and the baud for ASK, FSK, PSK, and QAM. Note that with the three binary modulation schemes (ASK, FSK, and

Table 1 ASK, FSK, PSK, and QAM Summary

Modulation	Encoding Scheme	Outputs Possible	Minimum Bandwidth	Baud
ASK	Single bit	2	f_b	f_b
FSK	Single bit	2	f_b	f_b
BPSK	Single bit	2	f_b	f_b
QPSK	Dibits	4	$f_b/2$	$f_b/2$
8-PSK	Tribits	8	$f_b/3$	$f_b/3$
8-QAM	Tribits	8	$f_b/3$	$f_b/3$
16-QAM	Quadbits	16	$f_b/4$	$f_b/4$
16-PSK	Quadbits	16	$f_b/4$	$f_b/4$
32-PSK	Five bits	32	$f_b/5$	$f_b/5$
32-QAM	Five bits	32	$f_b/5$	$f_b/5$
64-PSK	Six bits	64	$f_b/6$	$f_b/6$
64-QAM	Six bits	64	$f_b/6$	$f_b/6$
128-PSK	Seven bits	128	$f_b/7$	$f_b/7$
128-QAM	Seven bits	128	$f_b/7$	$f_b/7$

Note: f_b indicates a magnitude equal to the input bit rate.

BPSK), $n = 1$, $M = 2$, only two output conditions are possible, and the baud is equal to the bit rate. However, for values of $n > 1$, the number of output conditions increases, and the minimum bandwidth and baud decrease. Therefore, digital modulation schemes where $n > 1$ achieve *bandwidth compression* (i.e., less bandwidth is required to propagate a given bit rate). When data compression is performed, higher data transmission rates are possible for a given bandwidth.

7 BANDWIDTH EFFICIENCY

Bandwidth efficiency (sometimes called *information density* or *spectral efficiency*) is often used to compare the performance of one digital modulation technique to another. In essence, bandwidth efficiency is the ratio of the transmission bit rate to the minimum bandwidth required for a particular modulation scheme. Bandwidth efficiency is generally normalized to a 1-Hz bandwidth and, thus, indicates the number of bits that can be propagated through a transmission medium for each hertz of bandwidth. Mathematically, bandwidth efficiency is

$$B\eta = \frac{\text{transmission bit rate (bps)}}{\text{minimum bandwidth (Hz)}} \tag{27}$$

$$= \frac{\text{bits/s}}{\text{hertz}} = \frac{\text{bits/s}}{\text{cycles/s}} = \frac{\text{bits}}{\text{cycle}}$$

where $B\eta$ = bandwidth efficiency

Bandwidth efficiency can also be given as a percentage by simply multiplying $B\eta$ by 100.

Example 13

For an 8-PSK system, operating with an information bit rate of 24 kbps, determine (a) baud, (b) minimum bandwidth, and (c) bandwidth efficiency.

Solution **a.** Baud is determined by substituting into Equation 10:

$$\text{baud} = \frac{24{,}000}{3} = 8000$$

b. Bandwidth is determined by substituting into Equation 11:

$$B = \frac{24{,}000}{3} = 8000$$

c. Bandwidth efficiency is calculated from Equation 27:

$$B\eta = \frac{24{,}000 \text{ bps}}{8000 \text{ Hz}}$$

$$= 3 \text{ bits per second per cycle of bandwidth}$$

Example 14

For 16-PSK and a transmission system with a 10 kHz bandwidth, determine the maximum bit rate.

Solution The bandwidth efficiency for 16-PSK is 4, which means that four bits can be propagated through the system for each hertz of bandwidth. Therefore, the maximum bit rate is simply the product of the bandwidth and the bandwidth efficiency, or

$$\text{bit rate} = 4 \times 10{,}000$$

$$= 40{,}000 \text{ bps}$$

Table 2 ASK, FSK, PSK, and QAM Summary

Modulation	Encoding Scheme	Outputs Possible	Minimum Bandwidth	Baud	Bη
ASK	Single bit	2	f_b	f_b	1
FSK	Single bit	2	f_b	f_b	1
BPSK	Single bit	2	f_b	f_b	1
QPSK	Dibits	4	$f_b/2$	$f_b/2$	2
8-PSK	Tribits	8	$f_b/3$	$f_b/3$	3
8-QAM	Tribits	8	$f_b/3$	$f_b/3$	3
16-PSK	Quadbits	16	$f_b/4$	$f_b/4$	4
16-QAM	Quadbits	16	$f_b/4$	$f_b/4$	4
32-PSK	Five bits	32	$f_b/5$	$f_b/5$	5
64-QAM	Six bits	64	$f_b/6$	$f_b/6$	6

Note: f_b indicates a magnitude equal to the input bit rate.

7-1 Digital Modulation Summary

The properties of several digital modulation schemes are summarized in Table 2.

8 CARRIER RECOVERY

Carrier recovery is the process of extracting a phase-coherent reference carrier from a receiver signal. This is sometimes called *phase referencing.*

In the phase modulation techniques described thus far, the binary data were encoded as a precise phase of the transmitted carrier. (This is referred to as *absolute phase encoding.*) Depending on the encoding method, the angular separation between adjacent phasors varied between 30° and 180°. To correctly demodulate the data, a phase-coherent carrier was recovered and compared with the received carrier in a product detector. To determine the absolute phase of the received carrier, it is necessary to produce a carrier at the receiver that is phase coherent with the transmit reference oscillator. This is the function of the carrier recovery circuit.

With PSK and QAM, the carrier is suppressed in the balanced modulators and, therefore, is not transmitted. Consequently, at the receiver the carrier cannot simply be tracked with a standard phase-locked loop (PLL). With suppressed-carrier systems, such as PSK and QAM, sophisticated methods of carrier recovery are required, such as a *squaring loop,* a *Costas loop,* or a *remodulator.*

8-1 Squaring Loop

A common method of achieving carrier recovery for BPSK is the *squaring loop.* Figure 37 shows the block diagram of a squaring loop. The received BPSK waveform is filtered and then squared. The filtering reduces the spectral width of the received noise. The squaring circuit removes the modulation and generates the second harmonic of the carrier frequency. This harmonic is phase tracked by the PLL. The VCO output frequency from the PLL then is divided by 2 and used as the phase reference for the product detectors.

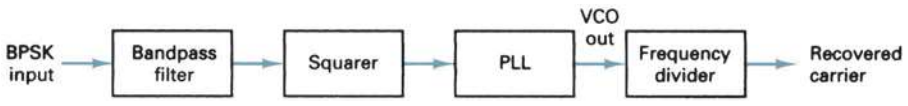


FIGURE 37 Squaring loop carrier recovery circuit for a BPSK receiver

With BPSK, only two output phases are possible: $+\sin \omega_c t$ and $-\sin \omega_c t$. Mathematically, the operation of the squaring circuit can be described as follows. For a receive signal of $+\sin \omega_c t$, the output of the squaring circuit is

$$\text{output} = (+\sin \omega_c t)(+\sin \omega_c t) = +\sin^2 \omega_c t$$

(filtered out)

$$= \frac{1}{2}(1 - \cos 2\omega_c t) = \frac{1}{2} - \frac{1}{2}\cos 2\omega_c t$$

For a received signal of $-\sin \omega_c t$, the output of the squaring circuit is

$$\text{output} = (-\sin \omega_c t)(-\sin \omega_c t) = +\sin^2 \omega_c t$$

(filtered out)

$$= \frac{1}{2}(1 - \cos 2\omega_c t) = \frac{1}{2} - \frac{1}{2}\cos 2\omega_c t$$

It can be seen that in both cases, the output from the squaring circuit contained a constant voltage (+1/2 V) and a signal at twice the carrier frequency ($\cos 2\omega_c t$). The constant voltage is removed by filtering, leaving only $\cos 2\omega_c t$.

8-2 Costas Loop

A second method of carrier recovery is the Costas, or quadrature, loop shown in Figure 38. The Costas loop produces the same results as a squaring circuit followed by an ordinary PLL in place of the BPF. This recovery scheme uses two parallel tracking loops (I and Q) simultaneously to derive the product of the I and Q components of the signal that drives the VCO. The in-phase (I) loop uses the VCO as in a PLL, and the quadrature (Q) loop uses a 90° shifted VCO signal. Once the frequency of the VCO is equal to the suppressed-carrier

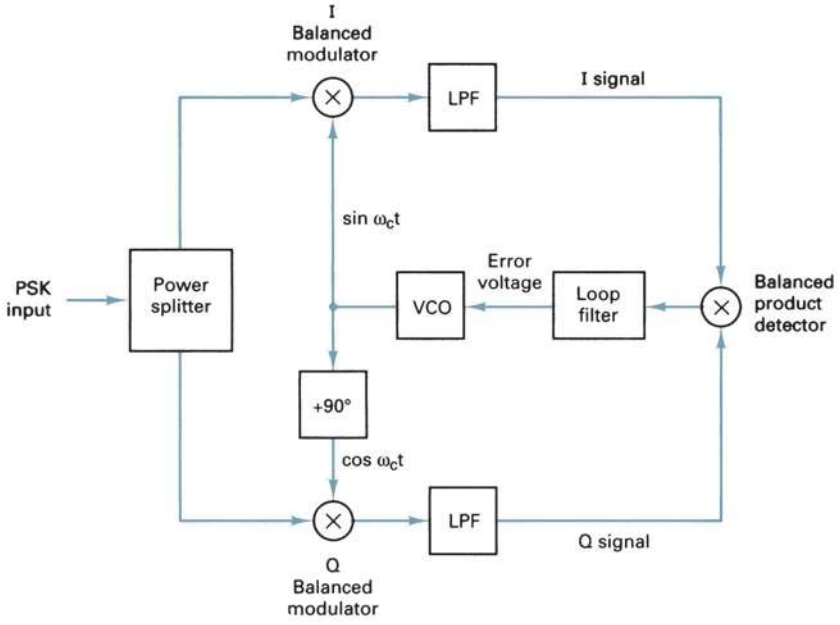


FIGURE 38 Costas loop carrier recovery circuit

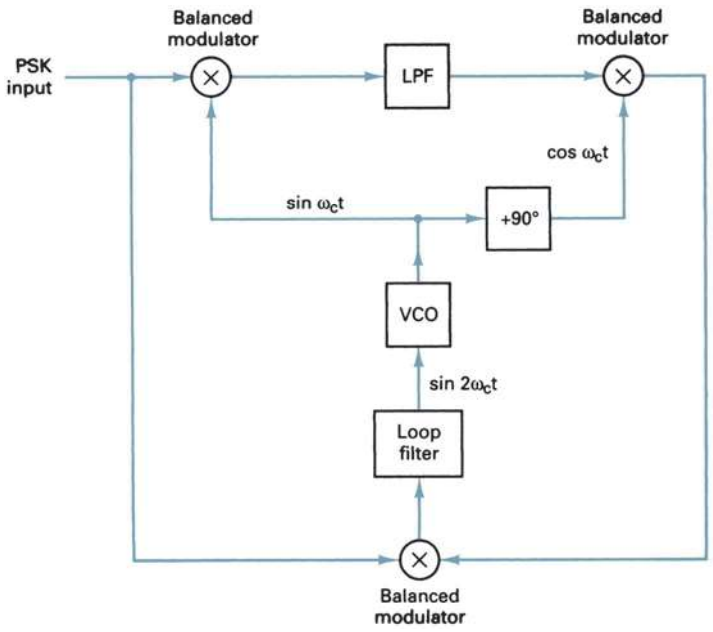


FIGURE 39 Remodulator loop carrier recovery circuit

frequency, the product of the I and Q signals will produce an error voltage proportional to any phase error in the VCO. The error voltage controls the phase and, thus, the frequency of the VCO.

8-3 Remodulator

A third method of achieving recovery of a phase and frequency coherent carrier is the remodulator, shown in Figure 39. The remodulator produces a loop error voltage that is proportional to twice the phase error between the incoming signal and the VCO signal. The remodulator has a faster acquisition time than either the squaring or the Costas loops.

Carrier recovery circuits for higher-than-binary encoding techniques are similar to BPSK except that circuits that raise the receive signal to the fourth, eighth, and higher powers are used.

9 CLOCK RECOVERY

As with any digital system, digital radio requires precise timing or clock synchronization between the transmit and the receive circuitry. Because of this, it is necessary to regenerate clocks at the receiver that are synchronous with those at the transmitter.

Figure 40a shows a simple circuit that is commonly used to recover clocking information from the received data. The recovered data are delayed by one-half a bit time and then compared with the original data in an XOR circuit. The frequency of the clock that is recovered with this method is equal to the received data rate (f_b). Figure 40b shows the relationship between the data and the recovered clock timing. From Figure 40b, it can be seen that as long as the receive data contain a substantial number of transitions (1/0 sequences), the recovered clock is maintained. If the receive data were to undergo an extended period of successive 1s or 0s, the recovered clock would be lost. To prevent this from occurring, the data are scrambled at the transmit end and descrambled at the receive end. Scrambling introduces transitions (pulses) into the binary signal using a prescribed algorithm, and the descrambler uses the same algorithm to remove the transitions.

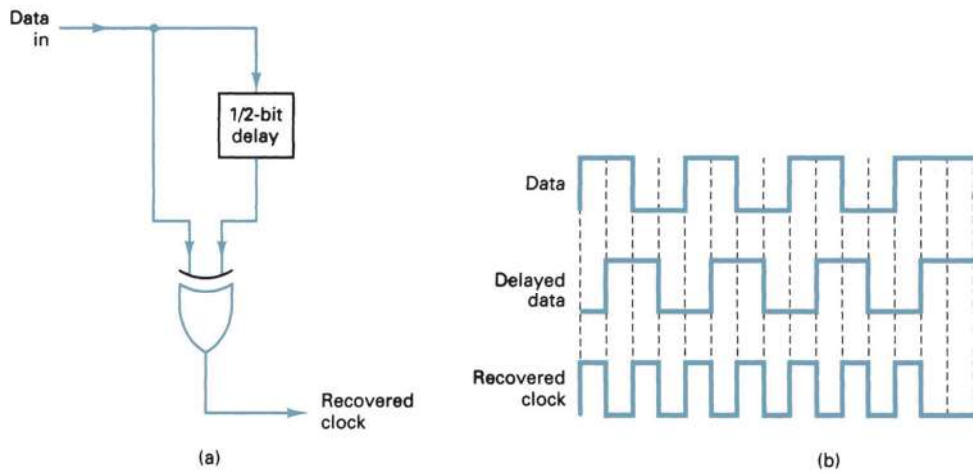


FIGURE 40 (a) Clock recovery circuit; (b) timing diagram

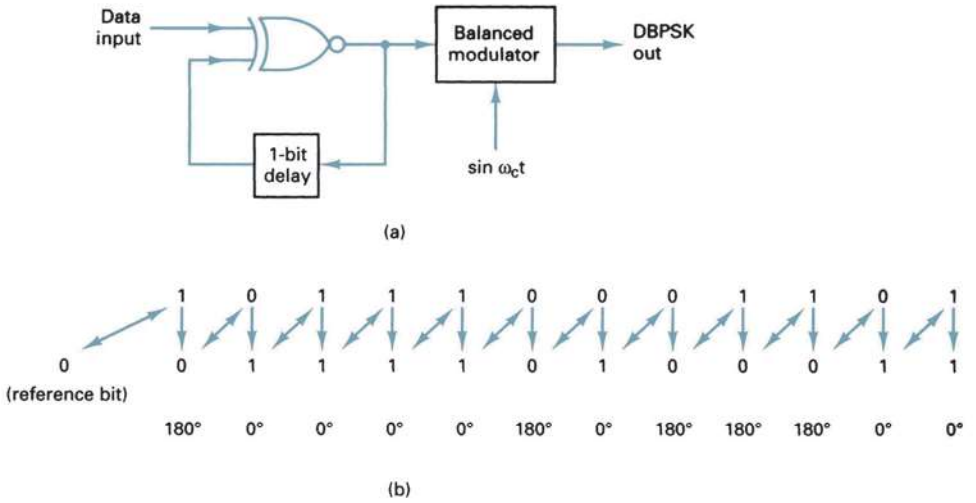


FIGURE 41 DBPSK modulator: (a) block diagram; (b) timing diagram

10 DIFFERENTIAL PHASE-SHIFT KEYING

Differential phase-shift keying (DPSK) is an alternative form of digital modulation where the binary input information is contained in the difference between two successive signaling elements rather than the absolute phase. With DPSK, it is not necessary to recover a phase-coherent carrier. Instead, a received signaling element is delayed by one signaling element time slot and then compared with the next received signaling element. The difference in the phase of the two signaling elements determines the logic condition of the data.

10-1 Differential BPSK

10-1-1 DBPSK transmitter. Figure 41a shows a simplified block diagram of a *differential binary phase-shift keying* (DBPSK) transmitter. An incoming information bit is

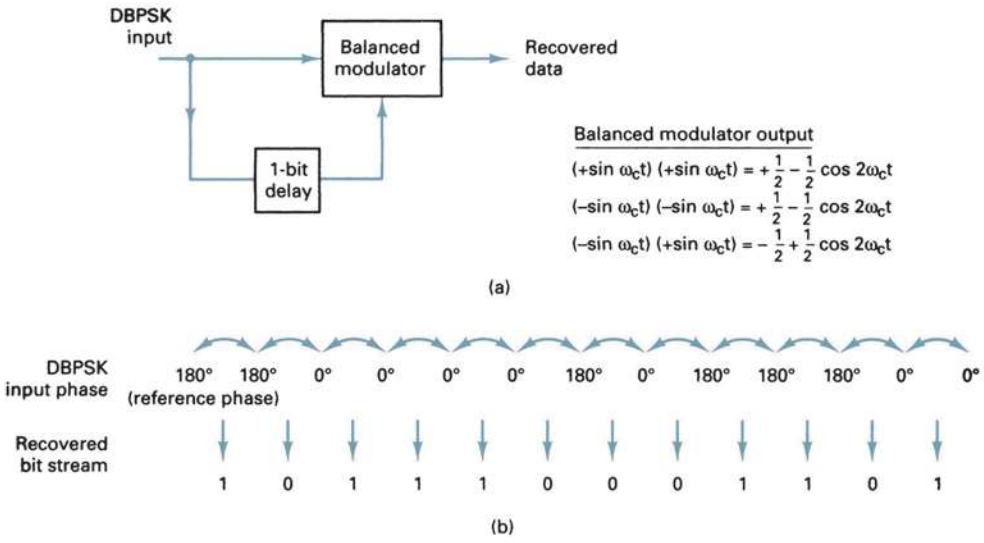


FIGURE 42 DBPSK demodulator: (a) block diagram; (b) timing sequence

XNORed with the preceding bit prior to entering the BPSK modulator (balanced modulator). For the first data bit, there is no preceding bit with which to compare it. Therefore, an initial reference bit is assumed. Figure 41b shows the relationship between the input data, the XNOR output data, and the phase at the output of the balanced modulator. If the initial reference bit is assumed a logic 1, the output from the XNOR circuit is simply the complement of that shown.

In Figure 41b, the first data bit is XNORed with the reference bit. If they are the same, the XNOR output is a logic 1; if they are different, the XNOR output is a logic 0. The balanced modulator operates the same as a conventional BPSK modulator; a logic 1 produces $+\sin \omega_c t$ at the output, and a logic 0 produces $-\sin \omega_c t$ at the output.

10-1-2 DBPSK receiver. Figure 42 shows the block diagram and timing sequence for a DBPSK receiver. The received signal is delayed by one bit time, then compared with the next signaling element in the balanced modulator. If they are the same, a logic 1 (+ voltage) is generated. If they are different, a logic 0 (− voltage) is generated. If the reference phase is incorrectly assumed, only the first demodulated bit is in error. Differential encoding can be implemented with higher-than-binary digital modulation schemes, although the differential algorithms are much more complicated than for DBPSK.

The primary advantage of DBPSK is the simplicity with which it can be implemented. With DBPSK, no carrier recovery circuit is needed. A disadvantage of DBPSK is that it requires between 1 dB and 3 dB more signal-to-noise ratio to achieve the same bit error rate as that of absolute PSK.

11 TRELLIS CODE MODULATION

Achieving data transmission rates in excess of 9600 bps over standard telephone lines with approximately a 3-kHz bandwidth obviously requires an encoding scheme well beyond the quadbits used with 16-PSK or 16-QAM (i.e., M must be significantly greater than 16). As might be expected, higher encoding schemes require higher signal-to-noise ratios. Using the Shannon limit for information capacity (Equation 4), a data transmission rate of 28.8 kbps through a 3200-Hz bandwidth requires a signal-to-noise ratio of

$$I(\text{bps}) = (3.32 \times B) \log(1 + \text{S/N})$$

therefore,

$$28.8 \text{ kbps} = (3.32)(3200)\log(1 + S/N)$$

$$28{,}800 = 10{,}624 \log(1 + S/N)$$

$$\frac{28{,}800}{10{,}624} = \log(1 + S/N)$$

$$2.71 = \log(1 + S/N)$$

thus,

$$10^{2.71} = 1 + S/N$$

$$513 = 1 + S/N$$

$$512 = S/N$$

in dB,

$$S/N_{(dB)} = 10 \log 512$$

$$= 27 \text{ dB}$$

Transmission rates of 56 kbps require a signal-to-noise ratio of 53 dB, which is virtually impossible to achieve over a standard telephone circuit.

Data transmission rates in excess of 56 kbps can be achieved, however, over standard telephone circuits using an encoding technique called *trellis code modulation* (TCM). Dr. Ungerboeck at IBM Zuerich Research Laboratory developed TCM, which involves using *convolutional* (*tree*) codes, which combines encoding and modulation to reduce the probability of error, thus improving the bit error performance. The fundamental idea behind TCM is introducing controlled redundancy in the bit stream with a convolutional code, which reduces the likelihood of transmission errors. What sets TCM apart from standard encoding schemes is the introduction of redundancy by doubling the number of signal points in a given PSK or QAM constellation.

Trellis code modulation is sometimes thought of as a magical method of increasing transmission bit rates over communications systems using QAM or PSK with fixed bandwidths. Few people fully understand this concept, as modem manufacturers do not seem willing to share information on TCM. Therefore, the following explanation is intended not to fully describe the process of TCM but rather to introduce the topic and give the reader a basic understanding of how TCM works and the advantage it has over conventional digital modulation techniques.

M-ary QAM and PSK utilize a signal set of $2^N = M$, where N equals the number of bits encoded into M different conditions. Therefore, $N = 2$ produces a standard PSK constellation with four signal points (i.e., QPSK) as shown in Figure 43a. Using TCM, the number of signal points increases to two times M possible symbols for the same factor-of-M reduction in bandwidth while transmitting each signal during the same time interval. TCM-encoded QPSK is shown in Figure 43b.

Trellis coding also defines the manner in which signal-state transitions are allowed to occur, and transitions that do not follow this pattern are interpreted in the receiver as transmission errors. Therefore, TCM can improve error performance by restricting the manner in which signals are allowed to transition. For values of N greater than 2, QAM is the modulation scheme of choice for TCM; however, for simplification purposes, the following explanation uses PSK as it is easier to illustrate.

Figure 44 shows a TCM scheme using two-state 8-PSK, which is essentially two QPSK constellations offset by 45°. One four-state constellation is labeled 0-4-2-6, and the other is labeled 1-5-3-7. For this explanation, the signal point labels 0 through 7 are meant not to represent the actual data conditions but rather to simply indicate a convenient method of labeling the various signal points. Each digit represents one of four signal points permitted within each of the two QPSK constellations. When in the 0-4-2-6 constellation and a 0 or 4 is transmitted, the system remains in the same constellation. However, when either a 2 or 6 is transmitted, the system switches to the 1-5-3-7 constellation. Once in the 1-5-3-7

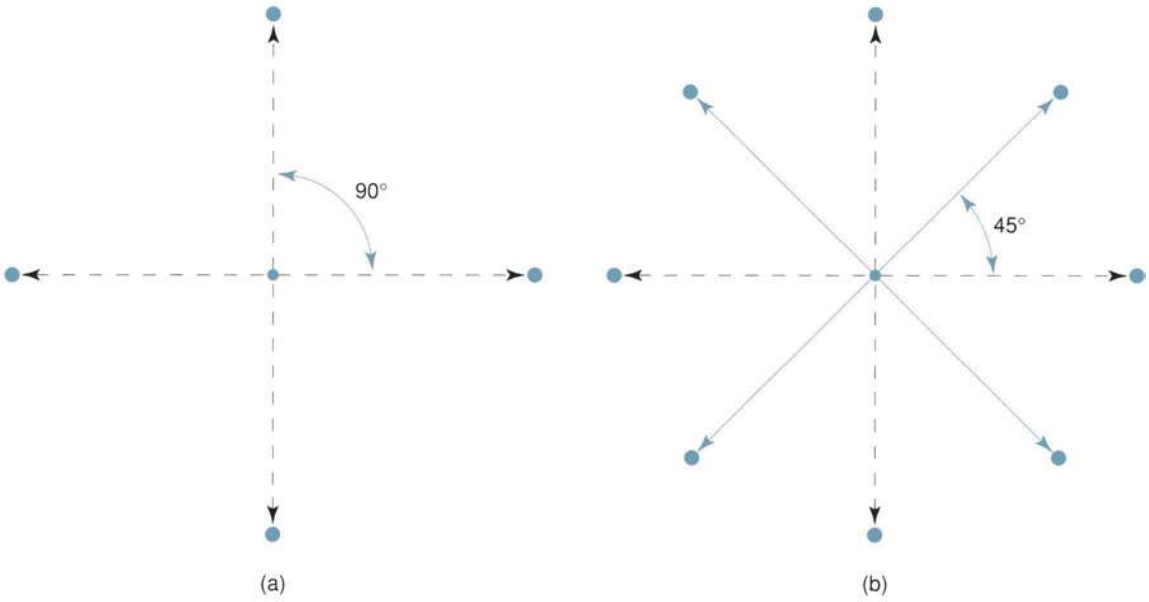


FIGURE 43 QPSK constellations: (a) standard encoding format; (b) trellis encoding format

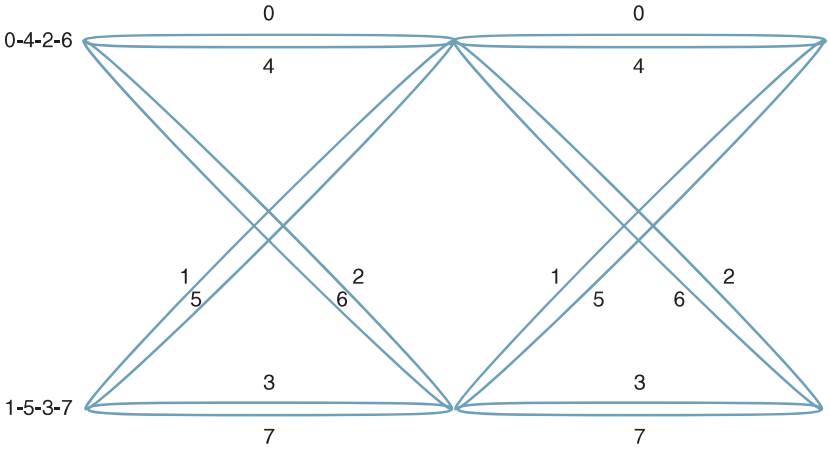


FIGURE 44 8-PSK TCM constellations

constellation and a 3 or 7 is transmitted, the system remains in the same constellation, and if a 1 or 5 is transmitted, the system switches to the 0-4-2-6 constellation. Remember that each symbol represents two bits, so the system undergoes a 45° phase shift whenever it switches between the two constellations. A complete error analysis of standard QPSK compared with TCM QPSK would reveal a coding gain for TCM of 2-to-1 1 or 3 dB. Table 3 lists the coding gains achieved for TCM coding schemes with several different trellis states.

The maximum data rate achievable using a given bandwidth can be determined by rearranging Equation 10:

$$N \times B = f_b$$

Table 3 Trellis Coding Gain

Number of Trellis States	Coding Gain (dB)
2	3.0
4	5.5
8	6.0
16	6.5
32	7.1
64	7.3
128	7.3
256	7.4

where N = number of bits encoded (bits)
B = bandwidth (hertz)
f_b = transmission bit rate (bits per second)

Remember that with M-ary QAM or PSK systems, the baud equals the minimum required bandwidth. Therefore, a 3200-Hz bandwidth using a nine-bit trellis code produces a 3200 baud signal with each baud carrying nine bits. Therefore, the transmission rate $f_b = 9 \times 3200 = 28.8$ kbps.

TCM is thought of as a coding scheme that improves on standard QAM by increasing the distance between symbols on the constellation (known as the *Euclidean distance*). The first TCM system used a five-bit code, which included four QAM bits (a quadbit) and a fifth bit used to help decode the quadbit. Transmitting five bits within a single signaling element requires producing 32 discernible signals. Figure 45 shows a 128-point QAM constallation.

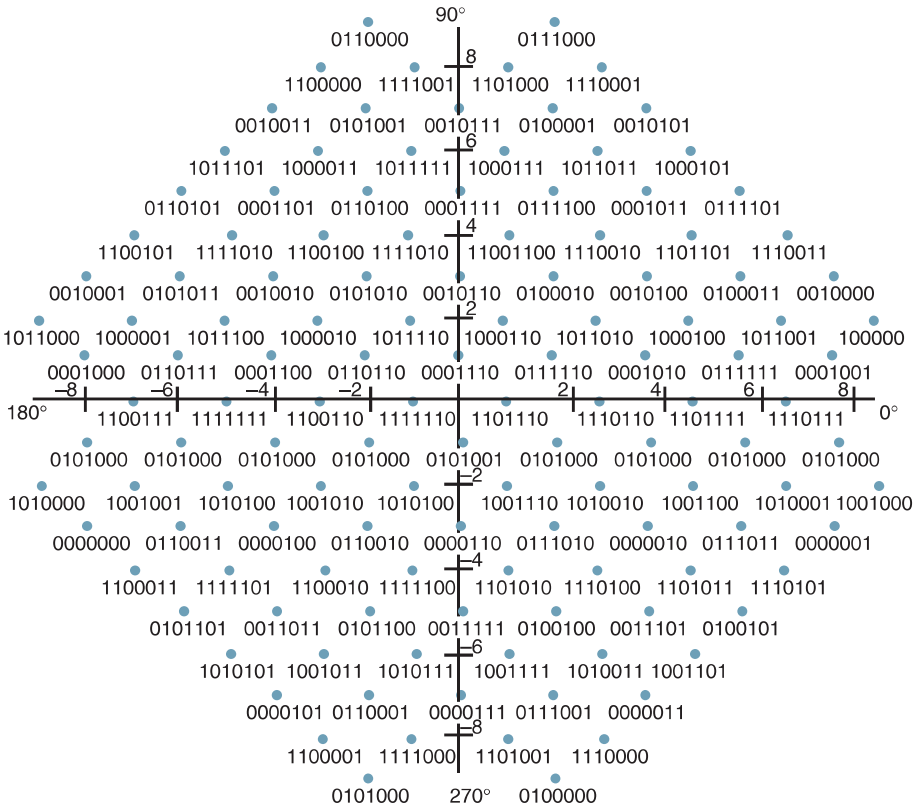


FIGURE 45 128-Point QAM TCM constellation

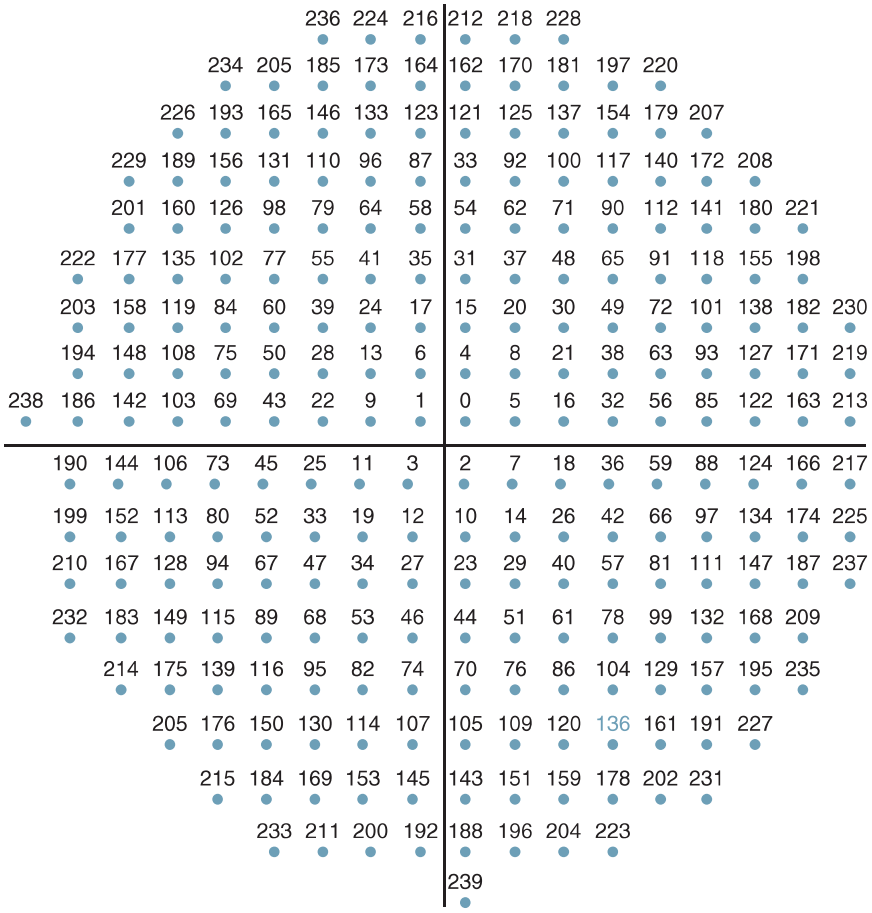


FIGURE 46 One-fourth of a 960-Point QAM TCM constellation

A 3200-baud signal using nine-bit TCM encoding produces 512 different codes. The nine data bits plus a redundant bit for TCM requires a 960-point constellation. Figure 46 shows one-fourth of the 960-point superconstellation showing 240 signal points. The full superconstellation can be obtained by rotating the 240 points shown by 90°, 180°, and 270°.

12 PROBABILITY OF ERROR AND BIT ERROR RATE

Probability of error $P(e)$ and *bit error rate* (BER) are often used interchangeably, although in practice they do have slightly different meanings. $P(e)$ is a theoretical (mathematical) expectation of the bit error rate for a given system. BER is an empirical (historical) record of a system's actual bit error performance. For example, if a system has a $P(e)$ of 10^{-5}, this means that mathematically you can expect one bit error in every 100,000 bits transmitted ($1/10^{-5} = 1/100{,}000$). If a system has a BER of 10^{-5}, this means that in past performance there was one bit error for every 100,000 bits transmitted. A bit error rate is measured and then compared with the expected probability of error to evaluate a system's performance.

Probability of error is a function of the *carrier-to-noise power ratio* (or, more specifically, the average *energy per bit-to-noise power density ratio*) and the number of possible encoding conditions used (*M*-ary). Carrier-to-noise power ratio is the ratio of the average carrier power (the combined power of the carrier and its associated sidebands) to the *thermal noise power.* Carrier power can be stated in watts or dBm, where

$$C_{(\text{dBm})} = 10 \log \frac{C_{(\text{watts})}}{0.001} \tag{28}$$

Thermal noise power is expressed mathematically as

$$N = KTB \text{ (watts)} \tag{29}$$

where N = thermal noise power (watts)
K = Boltzmann's proportionality constant (1.38×10^{-23} joules per kelvin)
T = temperature (kelvin: 0 K = −273° C, room temperature = 290 K)
B = bandwidth (hertz)

Stated in dBm,

$$N_{(\text{dBm})} = 10 \log \frac{KTB}{0.001} \tag{30}$$

Mathematically, the carrier-to-noise power ratio is

$$\frac{C}{N} = \frac{C}{KTB} \text{ (unitless ratio)} \tag{31}$$

where C = carrier power (watts)
N = noise power (watts)

Stated in dB,

$$\frac{C}{N}(\text{dB}) = 10 \log \frac{C}{N}$$

$$= C_{(\text{dBm})} - N_{(\text{dBm})} \tag{32}$$

Energy per bit is simply the energy of a single bit of information. Mathematically, energy per bit is

$$E_b = CT_b \text{ (J/bit)} \tag{33}$$

where E_b = energy of a single bit (joules per bit)
T_b = time of a single bit (seconds)
C = carrier power (watts)

Stated in dBJ,

$$E_{b(\text{dBJ})} = 10 \log E_b \tag{34}$$

and because $T_b = 1/f_b$, where f_b is the bit rate in bits per second, E_b can be rewritten as

$$E_b = \frac{C}{f_b} \text{ (J/bit)} \tag{35}$$

Stated in dBJ,

$$E_{b\,(\text{dBJ})} = 10 \log \frac{C}{f_b} \tag{36}$$

$$= 10 \log C - 10 \log f_b \tag{37}$$

Noise power density is the thermal noise power normalized to a 1-Hz bandwidth (i.e., the noise power present in a 1-Hz bandwidth). Mathematically, noise power density is

$$N_0 = \frac{N}{B}\,(\text{W/Hz}) \tag{38}$$

where N_0 = noise power density (watts per hertz)
N = thermal noise power (watts)
B = bandwidth (hertz)

Stated in dBm,
$$N_{0(\text{dBm})} = 10 \log \frac{N}{0.001} - 10 \log B \tag{39}$$
$$= N_{(\text{dBm})} - 10 \log B \tag{40}$$

Combining Equations 29 and 38 yields

$$N_0 = \frac{KTB}{B} = KT\,(\text{W/Hz}) \tag{41}$$

Stated in dBm,
$$N_{0(\text{dBm})} = 10 \log \frac{K}{0.001} + 10 \log T \tag{42}$$

Energy per bit-to-noise power density ratio is used to compare two or more digital modulation systems that use different transmission rates (bit rates), modulation schemes (FSK, PSK, QAM), or encoding techniques (M-ary). The energy per bit-to-noise power density ratio is simply the ratio of the energy of a single bit to the noise power present in 1 Hz of bandwidth. Thus, E_b/N_0 normalizes all multiphase modulation schemes to a common noise bandwidth, allowing for a simpler and more accurate comparison of their error performance. Mathematically, E_b/N_0 is

$$\frac{E_b}{N_0} = \frac{C/f_b}{N/B} = \frac{CB}{Nf_b} \tag{43}$$

where E_bN_0 is the energy per bit-to-noise power density ratio. Rearranging Equation 43 yields the following expression:

$$\frac{E_b}{N_0} = \frac{C}{N} \times \frac{B}{f_b} \tag{44}$$

where E_b/N_0 = energy per bit-to-noise power density ratio
C/N = carrier-to-noise power ratio
B/f_b = noise bandwidth-to-bit rate ratio

Stated in dB,
$$\frac{E_b}{N_0}\,(\text{dB}) = 10 \log \frac{C}{N} + 10 \log \frac{B}{f_b} \tag{45}$$
or
$$= 10 \log E_b - 10 \log N_0 \tag{46}$$

From Equation 44, it can be seen that the E_b/N_0 ratio is simply the product of the carrier-to-noise power ratio and the noise bandwidth-to-bit rate ratio. Also, from Equation 44, it can be seen that when the bandwidth equals the bit rate, $E_b/N_0 = C/N$.

In general, the minimum carrier-to-noise power ratio required for QAM systems is less than that required for comparable PSK systems, Also, the higher the level of encoding used (the higher the value of M), the higher the minimum carrier-to-noise power ratio.

Example 15

For a QPSK system and the given parameters, determine

a. Carrier power in dBm.
b. Noise power in dBm.

c. Noise power density in dBm.
d. Energy per bit in dBJ.
e. Carrier-to-noise power ratio in dB.
f. E_b/N_0 ratio.

$$C = 10^{-12}\ \text{W} \qquad f_b = 60\ \text{kbps}$$
$$N = 1.2 \times 10^{-14}\ \text{W} \qquad B = 120\ \text{kHz}$$

Solution a. The carrier power in dBm is determined by substituting into Equation 28:

$$C = 10 \log \frac{10^{-12}}{0.001} = -90\ \text{dBm}$$

b. The noise power in dBm is determined by substituting into Equation 30:

$$N = 10 \log \frac{1.2 \times 10^{-14}}{0.001} = -109.2\ \text{dBm}$$

c. The noise power density is determined by substituting into Equation 40:

$$N_0 = -109.2\ \text{dBm} - 10 \log 120\ \text{kHz} = -160\ \text{dBm}$$

d. The energy per bit is determined by substituting into Equation 36:

$$E_b = 10 \log \frac{10^{-12}}{60\ \text{kbps}} = -167.8\ \text{dBJ}$$

e. The carrier-to-noise power ratio is determined by substituting into Equation 34:

$$\frac{C}{N} = 10 \log \frac{10^{-12}}{1.2 \times 10^{-14}} = 19.2\ \text{dB}$$

f. The energy per bit-to-noise density ratio is determined by substituting into Equation 45:

$$\frac{E_b}{N_0} = 19.2 + 10 \log \frac{120\ \text{kHz}}{60\ \text{kbps}} = 22.2\ \text{dB}$$

13 ERROR PERFORMANCE

13-1 PSK Error Performance

The bit error performance for the various multiphase digital modulation systems is directly related to the distance between points on a signal state-space diagram. For example, on the signal state-space diagram for BPSK shown in Figure 47a, it can be seen that the two signal points (logic 1 and logic 0) have maximum separation (d) for a given power level (D). In essence, one BPSK signal state is the exact negative of the other. As the figure shows, a noise vector (V_N), when combined with the signal vector (V_S), effectively shifts the phase of the signaling element (V_{SE}) alpha degrees. If the phase shift exceeds $\pm 90^\circ$, the signal element is shifted beyond the threshold points into the error region. For BPSK, it would require a noise vector of sufficient amplitude and phase to produce more than a $\pm 90^\circ$ phase shift in the signaling element to produce an error. For PSK systems, the general formula for the threshold points is

$$\text{TP} = \pm \frac{\pi}{M} \tag{47}$$

where M is the number of signal states.

The phase relationship between signaling elements for BPSK (i.e., 180° out of phase) is the optimum signaling format, referred to as *antipodal signaling,* and occurs only when two binary signal levels are allowed and when one signal is the exact negative of the other. Because no other bit-by-bit signaling scheme is any better, antipodal performance is often used as a reference for comparison.

The error performance of the other multiphase PSK systems can be compared with that of BPSK simply by determining the relative decrease in error distance between points

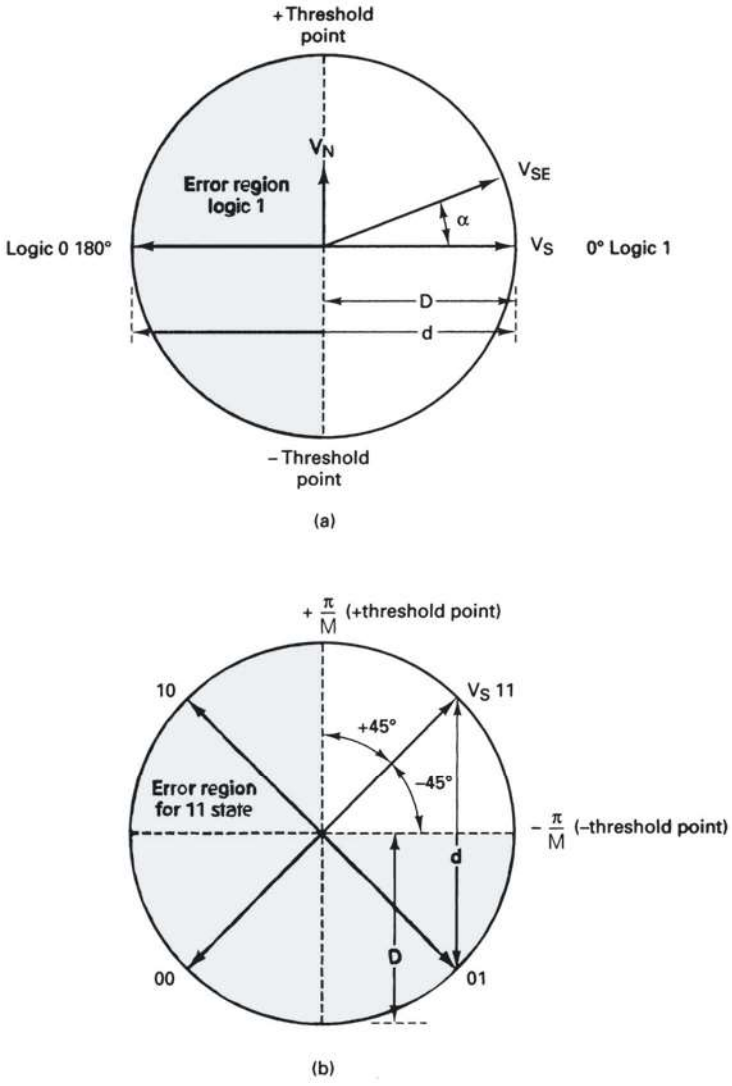


FIGURE 47 PSK error region: (a) BPSK; (b) QPSK

on a signal state-space diagram. For PSK, the general formula for the maximum distance between signaling points is given by

$$\sin\theta = \sin\frac{360^\circ}{2M} = \frac{d/2}{D} \tag{48}$$

where d = error distance
M = number of phases
D = peak signal amplitude

Rearranging Equation 48 and solving for d yields

$$d = \left(2\sin\frac{180^\circ}{M}\right) \times D \tag{49}$$

Figure 47b shows the signal state-space diagram for QPSK. From Figure 47 and Equation 48, it can be seen that QPSK can tolerate only a ±45° phase shift. From Equation 47,

the maximum phase shift for 8-PSK and 16-PSK is ±22.5° and ±11.25°, respectively. Consequently, the higher levels of modulation (i.e., the greater the value of M) require a greater energy per bit-to-noise power density ratio to reduce the effect of noise interference. Hence, the higher the level of modulation, the smaller the angular separation between signal points and the smaller the error distance.

The general expression for the bit error probability of an M-phase PSK system is

$$P(e) = \frac{1}{\log_2 M} \operatorname{erf}(z) \tag{50}$$

where erf = error function

$$z = \sin(\pi/M)(\sqrt{\log_2 M})(\sqrt{E_b/N_0})$$

By substituting into Equation 50, it can be shown that QPSK provides the same error performance as BPSK. This is because the 3-dB reduction in error distance for QPSK is offset by the 3-dB decrease in its bandwidth (in addition to the error distance, the relative widths of the noise bandwidths must also be considered). Thus, both systems provide optimum performance. Figure 48 shows the error performance for 2-, 4-, 8-, 16-, and 32-PSK systems as a function of E_b/N_0.

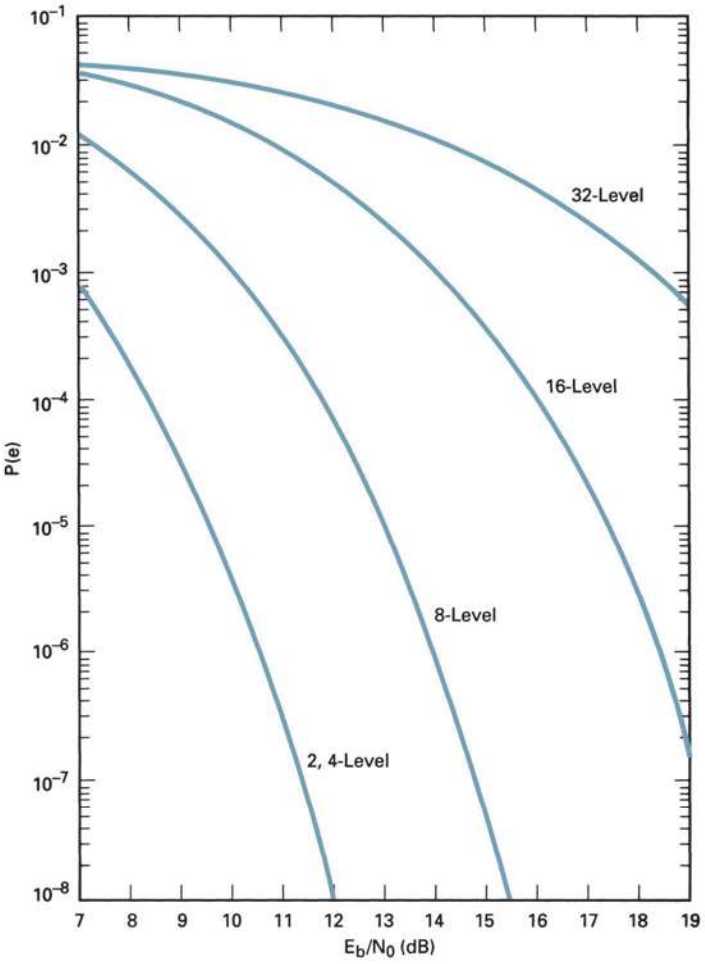


FIGURE 48 Error rates of PSK modulation systems

Example 16

Determine the minimum bandwidth required to achieve a $P(e)$ of 10^{-7} for an 8-PSK system operating at 10 Mbps with a carrier-to-noise power ratio of 11.7 dB.

Solution From Figure 48, the minimum E_b/N_0 ratio to achieve a $P(e)$ of 10^{-7} for an 8-PSK system is 14.7 dB. The minimum bandwidth is found by rearranging Equation 44:

$$\frac{B}{f_b} = \frac{E_b}{N_0} - \frac{C}{N}$$

$$= 14.7 \text{ dB} - 11.7 \text{ dB} = 3 \text{ dB}$$

$$\frac{B}{f_b} = \text{antilog } 3 = 2$$

$$B = 2 \times 10 \text{ Mbps} = 20 \text{ MHz}$$

13-2 QAM Error Performance

For a large number of signal points (i.e., M-ary systems greater than 4), QAM outperforms PSK. This is because the distance between signaling points in a PSK system is smaller than the distance between points in a comparable QAM system. The general expression for the distance between adjacent signaling points for a QAM system with L levels on each axis is

$$d = \frac{\sqrt{2}}{L-1} \times D \tag{51}$$

where d = error distance
L = number of levels on each axis
D = peak signal amplitude

In comparing Equation 49 to Equation 51, it can be seen that QAM systems have an advantage over PSK systems with the same peak signal power level.

The general expression for the bit error probability of an L-level QAM system is

$$P(e) = \frac{1}{\log_2 L}\left(\frac{L-1}{L}\right)\text{erfc}(z) \tag{52}$$

where erfc(z) is the complementary error function.

$$z = \frac{\sqrt{\log_2 L}}{L-1}\sqrt{\frac{E_b}{N_0}}$$

Figure 49 shows the error performance for 4-, 16-, 32-, and 64-QAM systems as a function of E_b/N_0.

Table 4 lists the minimum carrier-to-noise power ratios and energy per bit-to-noise power density ratios required for a probability of error 10^{-6} for several PSK and QAM modulation schemes.

Example 17

Which system requires the highest E_b/N_0 ratio for a probability of error of 10^{-6}, a four-level QAM system or an 8-PSK system?

Solution From Figure 49, the minimum E_b/N_0 ratio required for a four-level QAM system is 10.6 dB. From Figure 48, the minimum E_b/N_0 ratio required for an 8-PSK system is 14 dB. Therefore, to achieve a $P(e)$ of 10^{-6}, a four-level QAM system would require 3.4 dB less E_b/N_0 ratio.

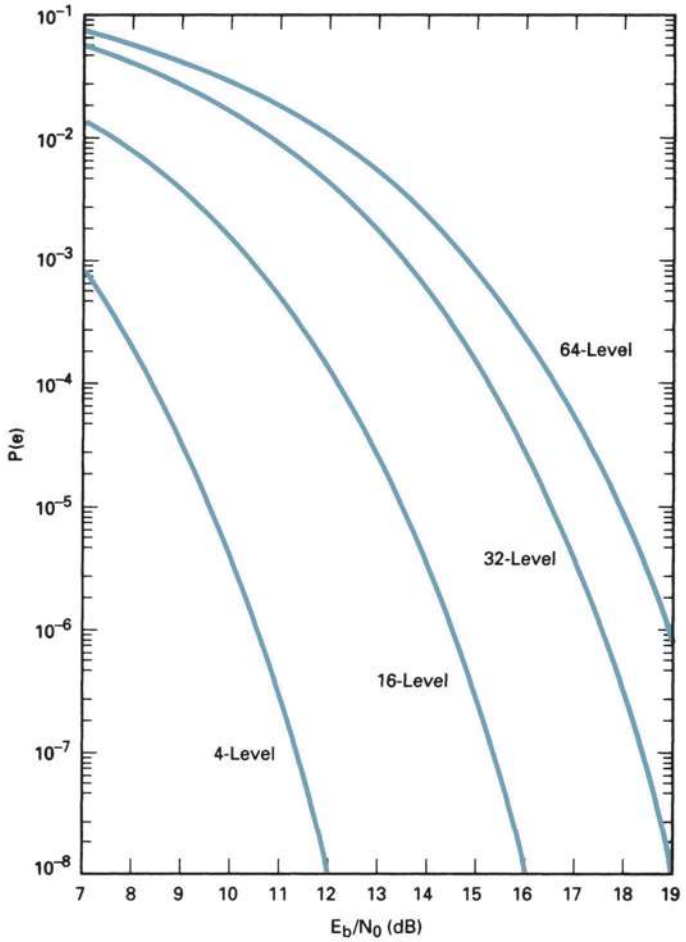


FIGURE 49 Error rates of QAM modulation systems

Table 4 Performance Comparison of Various Digital Modulation Schemes (BER = 10^{-6})

Modulation Technique	C/N Ratio (dB)	E_b/N_0 Ratio (dB)
BPSK	10.6	10.6
QPSK	13.6	10.6
4-QAM	13.6	10.6
8-QAM	17.6	10.6
8-PSK	18.5	14
16-PSK	24.3	18.3
16-QAM	20.5	14.5
32-QAM	24.4	17.4
64-QAM	26.6	18.8

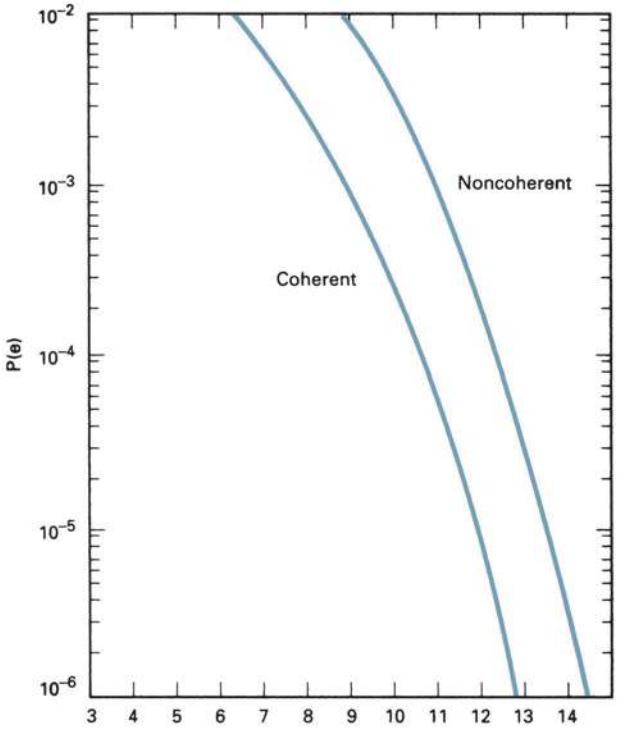


FIGURE 50 Error rates for FSK modulation systems

13-3 FSK Error Performance

The error probability for FSK systems is evaluated in a somewhat different manner than PSK and QAM. There are essentially only two types of FSK systems: noncoherent (asynchronous) and coherent (synchronous). With noncoherent FSK, the transmitter and receiver are not frequency or phase synchronized. With coherent FSK, local receiver reference signals are in frequency and phase lock with the transmitted signals. The probability of error for noncoherent FSK is

$$P(e) = \frac{1}{2}\exp\left(-\frac{E_b}{2N_0}\right) \tag{53}$$

The probability of error for coherent FSK is

$$P(e) = \operatorname{erfc}\sqrt{\frac{E_b}{N_0}} \tag{54}$$

Figure 50 shows probability of error curves for both coherent and noncoherent FSK for several values of E_b/N_0. From Equations 53 and 54, it can be determined that the probability of error for noncoherent FSK is greater than that of coherent FSK for equal energy per bit-to-noise power density ratios.

QUESTIONS

1. Explain *digital transmission* and *digital radio.*
2. Define *information capacity.*
3. What are the three most predominant modulation schemes used in digital radio systems?

4. Explain the relationship between bits per second and baud for an FSK system.
5. Define the following terms for FSK modulation: *frequency deviation, modulation index,* and *deviation ratio.*
6. Explain the relationship between (a) the minimum bandwidth required for an FSK system and the bit rate and (b) the mark and space frequencies.
7. What is the difference between standard FSK and MSK? What is the advantage of MSK?
8. Define *PSK.*
9. Explain the relationship between bits per second and baud for a BPSK system.
10. What is a constellation diagram, and how is it used with PSK?
11. Explain the relationship between the minimum bandwidth required for a BPSK system and the bit rate.
12. Explain *M*-ary.
13. Explain the relationship between bits per second and baud for a QPSK system.
14. Explain the significance of the I and Q channels in a QPSK modulator.
15. Define *dibit.*
16. Explain the relationship between the minimum bandwidth required for a QPSK system and the bit rate.
17. What is a coherent demodulator?
18. What advantage does OQPSK have over conventional QPSK? What is a disadvantage of OQPSK?
19. Explain the relationship between bits per second and baud for an 8-PSK system.
20. Define *tribit.*
21. Explain the relationship between the minimum bandwidth required for an 8-PSK system and the bit rate.
22. Explain the relationship between bits per second and baud for a 16-PSK system.
23. Define *quadbit.*
24. Define *QAM.*
25. Explain the relationship between the minimum bandwidth required for a 16-QAM system and the bit rate.
26. What is the difference between PSK and QAM?
27. Define *bandwidth efficiency.*
28. Define *carrier recovery.*
29. Explain the differences between absolute PSK and differential PSK.
30. What is the purpose of a clock recovery circuit? When is it used?
31. What is the difference between probability of error and bit error rate?

PROBLEMS

1. Determine the bandwidth and baud for an FSK signal with a mark frequency of 32 kHz, a space frequency of 24 kHz, and a bit rate of 4 kbps.
2. Determine the maximum bit rate for an FSK signal with a mark frequency of 48 kHz, a space frequency of 52 kHz, and an available bandwidth of 10 kHz.
3. Determine the bandwidth and baud for an FSK signal with a mark frequency of 99 kHz, a space frequency of 101 kHz, and a bit rate of 10 kbps.
4. Determine the maximum bit rate for an FSK signal with a mark frequency of 102 kHz, a space frequency of 104 kHz, and an available bandwidth of 8 kHz.
5. Determine the minimum bandwidth and baud for a BPSK modulator with a carrier frequency of 40 MHz and an input bit rate of 500 kbps. Sketch the output spectrum.
6. For the QPSK modulator shown in Figure 17, change the $+90°$ phase-shift network to $-90°$ and sketch the new constellation diagram.
7. For the QPSK demodulator shown in Figure 21, determine the I and Q bits for an input signal of $\sin \omega_c t - \cos \omega_c t$.

8. For an 8-PSK modulator with an input data rate (f_b) equal to 20 Mbps and a carrier frequency of 100 MHz, determine the minimum double-sided Nyquist bandwidth (f_N) and the baud. Sketch the output spectrum.
9. For the 8-PSK modulator shown in Figure 23, change the reference oscillator to cos $\omega_c t$ and sketch the new constellation diagram.
10. For a 16-QAM modulator with an input bit rate (f_b) equal to 20 Mbps and a carrier frequency of 100 MHz, determine the minimum double-sided Nyquist bandwidth (f_N) and the baud. Sketch the output spectrum.
11. For the 16-QAM modulator shown in Figure 33, change the reference oscillator to cos $\omega_c t$ and determine the output expressions for the following I, I′, Q, and Q′ input conditions: 0000, 1111, 1010, and 0101.
12. Determine the bandwidth efficiency for the following modulators:
    a. QPSK, $f_b = 10$ Mbps
    b. 8-PSK, $f_b = 21$ Mbps
    c. 16-QAM, $f_b = 20$ Mbps
13. For the DBPSK modulator shown in Figure 40a, determine the output phase sequence for the following input bit sequence: 00110011010101 (assume that the reference bit = 1).
14. For a QPSK system and the given parameters, determine
    a. Carrier power in dBm.
    b. Noise power in dBm.
    c. Noise power density in dBm.
    d. Energy per bit in dBJ.
    e. Carrier-to-noise power ratio.
    f. E_b/N_0 ratio.

    $C = 10^{-13}$ W $\quad f_b = 30$ kbps
    $N = 0.06 \times 10^{-15}$ W $\quad B = 60$ kHz
15. Determine the minimum bandwidth required to achieve a $P(e)$ of 10^{-6} for an 8-PSK system operating at 20 Mbps with a carrier-to-noise power ratio of 11 dB.
16. Determine the minimum bandwidth and baud for a BPSK modulator with a carrier frequency of 80 MHz and an input bit rate $f_b = 1$ Mbps. Sketch the output spectrum.
17. For the QPSK modulator shown in Figure 17, change the reference oscillator to cos $\omega_c t$ and sketch the new constellation diagram.
18. For the QPSK demodulator shown in Figure 21, determine the I and Q bits for an input signal $-\sin \omega_c t + \cos \omega_c t$.
19. For an 8-PSK modulator with an input bit rate $f_b = 10$ Mbps and a carrier frequency $f_c = 80$ MHz, determine the minimum Nyquist bandwidth and the baud. Sketch the output spectrum.
20. For the 8-PSK modulator shown in Figure 23, change the $+90°$ phase-shift network to a $-90°$ phase shifter and sketch the new constellation diagram.
21. For a 16-QAM modulator with an input bit rate $f_b = 10$ Mbps and a carrier frequency $f_c = 60$ MHz, determine the minimum double-sided Nyquist frequency and the baud. Sketch the output spectrum.
22. For the 16-QAM modulator shown in Figure 33, change the 90° phase shift network to a $-$ 90° phase shifter and determine the output expressions for the following I, I′, Q, and Q′ input conditions: 0000, 1111, 1010, and 0101.
23. Determine the bandwidth efficiency for the following modulators:
    a. QPSK, $f_b = 20$ Mbps
    b. 8-PSK, $f_b = 28$ Mbps
    c. 16-PSK, $f_b = 40$ Mbps
24. For the DBPSK modulator shown in Figure 40a, determine the output phase sequence for the following input bit sequence: 11001100101010 (assume that the reference bit is a logic 1).

ANSWERS TO SELECTED PROBLEMS

1. 16 kHz, 4000 baud
3. 22 kHz, 10 kbaud
5. 5 MHz, 5 Mbaud
7. I = 1, Q = 0
9.

Q	*I*	*C*	Phase
0	0	0	−22.5°
0	0	1	−67.5°
0	1	0	22.5°
0	1	1	67.5°
1	0	0	−157.5°
1	0	1	−112.5°
1	1	0	157.5°
1	1	1	112.5°

11.

Q	*Q'*	*I*	*I'*	Phase
0	0	0	0	−45°
1	1	1	1	135°
1	0	1	0	135°
0	1	0	1	−45°

13. Input 00110011010101
    XNOR 101110111001100
15. 40 MHz
17.

Q	*I*	Phase
0	0	−135°
0	1	−45°
1	0	135°
1	1	45°

19. 3.33 MHz, 3.33 Mbaud
21. 2.5 MHz, 2.5 Mbaud
23. a. 2 bps/Hz
    b. 3 bps/Hz
    c. 4 bps/Hz